Universal Instruments Corporation

Surface Mount Technology Laboratory

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Area Array 2001 Study Proposal

Executive Summary

The year 2000 was a dramatic one for the electronic industry. Explosive growth in the Contract Manufacturing Industry posed significant challenges for OEM's, CEM's and their suppliers. New component and material innovation demanded substantial assembly method development. Environmental and legislative pressures resulted in the need to implement a strategy for removing lead and bromine from the electronic production environment. Additionally optoelectronics has become prevalent on telecommunication and router boards. A clear requirement of this type of advancement is a fundamental understanding of the material, environmental and process interactions. Our development efforts in the past five Consortia studies have been focused on providing a fundamental understanding of the processes and materials that are used in a production environment. It is the goal of this study to continue and advance that understanding by studying the new materials, packages and processes that are becoming available. Continuity is served through continued development on BGA, CSP, WSP, DCA and microvia PCB's.

Project Goals

The principal goal of this Consortium is to provide fully documented processes, which can be used to produce high quality product at high yields. The work will be conducted in a systematic, logical and scientific manner with supporting documentation contributing adequate test data to allow reproducible results in a manufacturing environment. The data will be compiled in a CD ROM format.

Particular attention will be paid to determining why material systems and processes work. A specific effort will be undertaken to better understand the chemical interactions of the various material systems. This will allow the effective transfer of the process to other related products.

This test plan was prepared by the SMT Laboratory of Universal Instruments Corporation in Binghamton, NY, and reflects the needs of the participating firms through interactive review of the proposed plan with the Principals.

Consortium Structure

Two types of companies, Principals and Participants will support the Consortium. A Principal is a corporation that provides financial support to the Consortium process development and receives a complete copy of the test reports and final process documentation. A Principal is also encouraged to identify an individual to work or observe at Universal Instruments SMT Laboratory. Several Principals products will be selected as focused work efforts.

A Participant is a corporation that does not contribute financial support for the process development, but provides material and product development to the Consortium. A Participant will receive a report covering his own materials and a summary of its relative quality. No proprietary information pertaining to competitive Participants involved in the study will be communicated verbally or in writing to other Participants in the study.

Where ever possible we will attempt to utilize properly supported data generated by Principals, Participants or other reputable sources. A specific attempt will be made to focus our research into channels that have not been addressed sufficiently by the Principals. The following document does contain elements that have been investigated by more than one of the principals however we anticipate that some of the data covering these issues will be made available to the Consortium.

While the majority of the work will be focused in the SMT Laboratory of Universal Instruments Corp., some of the more esoteric or theoretical work may be subcontracted to Binghamton University, Clarkson, University of Southern California Santa Barbara, RPI, or Cornell University. It is also expected that participating consortium members who have unique expertise may perform some of the work.

We will form a close relationship with other consortia to help provide some of the supporting information on the various No-Lead assembly alloys.

Deliverables

The following technical topics are a natural outgrowth of the continued development of these packaging technologies within the past consortium as well as developments in the industry as a whole. These topics have been identified as those of greatest interest to the current Consortium Principals and were identified as a result of private discussions with industry experts within and outside the Consortium.

CSP Development Activity

The Year 2001 Consortium program will be focused on several key areas of activity. While most activities are related to area array package technology, some topics such as lead free solder and optoelectronics research, will extend into all areas of SMT and through hole technology. After a thorough review of packaging literature and discussions with key customers, the following areas of study have been identified for topics in the Area Array portion of the 2001 research consortia.

High Density Chip Scale Packages

High density chip scale packages in I/O count of 200+, will be thoroughly evaluated to provide a robust assembly process and second level assembly reliability data. Packages have been acquired in 1.0 to 0.5 mm pitch in pin counts of 4 I/O to 672 I/O. Development will include all relevant aspects of assembly including, printing, placement, and reflow. Component characterization will include first level tests when applicable. Moisture sensitivity at standard and lead free temperatures will be performed as well as determination of adequate bake times for moisture removal. Determination of critical package features such as ball diameter variations, are required to estimate assembly yields and assist in reliability predictions. Assembly of high density devices will be performed on a variety of pad finishes including lead free surfaces. Reliability testing will be performed on packages assembled using various experimental parameters including; attachment pad size, reflow atmosphere, paste type, pad finish, and board construction. Failure analysis will be provided for each type of package and each type of failure mode encountered. Destructive and non-destructive tests will be performed to characterize the assembly quality and solder joint shape.

CSP Repair

The need to repair high density area array devices requires a thorough investigation into the necessary steps of package rework. Critical process details as well as a determination of the reliability of reworked packages will be addressed. Detailed evaluation of process steps will include thermal profile development, package removal, site preparation, solder or flux application, and package replacement. In particular, site dressing of fine pitch devices, and sites with via in pad technology will be scrutinized. Damage to boards including mask removal and pad lifting have been reported in literature when redressing fine pitch CSP sites. Attention will be placed on methods for removal of residual solder that minimize or eliminate board damage. Evaluation of the reliability of the reworked site will be provided to ensure that components or boards are not compromised during the repair cycle.

Underfill for CSP

In addition to large CSP devices, smaller packages, often used in portable electronic devices, will be assessed. Special requirements for portable electronics such as drop and shock resistance, has forced the need to investigate both dispensed encapsulant and reflowable underfill and for CSP devices. Process parameters for dispensing and curing underfill for packaged die will be developed. In applications that require an increased mechanical reliability, for example, bending or twisting of the circuit card, partial underfill may be sufficient to increase the package handling robustness. In addition, underfill may change the thermal fatigue resistance of the component. Underfilled and non-underfilled assemblies will be compared.

Stacked Die CSP

CSP devices containing multiple die stacked on top of each other have become an additional area of interest, especially in memory devices where various SRAM and D-RAM die are being merged into a single package. BGA and CSPs are being developed that contain as many as three die within a single package. While multi-chip modules have been available on the market for many years, the stacked die utilize a different geometric arrangement of the silicon. In multi-chip modules the die are in the same X-Y plane, while in stacked die packages, the silicon is placed on top of a larger die. Many of these devices use a multi-tier wirebonding scheme to interconnect to a lead frame or component carrier. The effect of having more than one silicon layer within the die needs to be investigated. These devices will be included as part of the CSP development.

High Density Circuit Boards

Miniaturization of components has also driven circuit board manufacturers to shrink circuit features to accommodate the finer pitch parts. Board technology for components, flip chip area arrays, and motherboards will be explored in the program. High density via technology and routing methodology continues to be of primary interest in the assembly industry. Therefore, a goal of this program will be to evaluate high density PCB structures and create design guidelines and assembly process guides to assist manufacturers in implementing the new technology. The design guidelines may include routing methods for high density packages, via in pad recommendations, area array pad design footprints, as well as pad sizes for leadless and micro-lead frame devices. Evaluation of technology for both component carriers and mother board applications will be included.

Codification

Codification or documentation of the results will be presented in an electronic software database being developed for the Consortium members. Thousands of pictures, drawings, reliability plots, design rules and component test results will be included in a user friendly computer package. The goal of the software development will be to guide users through each step of the manufacturing process including design, component and board technology, prediction of process yields, and estimates on resulting assembly reliability. Individual modules for components, circuit boards, yield prediction, and reliability will be linked together to provide the user with as detailed a process tool as possible. The software will be modular in format and can be updated by the user to include assembly and materials information existing at each manufacturer or end users facility.

Lead Free

As the industry moves towards elimination of lead from electronics, a complete understanding of the materials, process, and reliability concerns must be determined for the alloys being considered. Primarily, silver, copper, and bismuth alloys are being evaluated by the industry for a suitable tin-lead solder replacement. These alloys and others will be included in the year 2001 Consortium research. Development will be focused on traditional surface mount devices as well as area array, and through hole technology. Area array component development in lead free will include determination of key reliability attributes. Specific properties such as crack propagation growth rates, and thermal cycle fatigue resistance will be sought for selected alloys. Development for surface mount packages will include traditional leaded devices and chip-capacitor / resistor components. While many of these components are being developed for lead free soldering, existing devices may be used in the transition period or during lead free phase in. Therefore, contamination of lead free solder with some amounts of lead (for example 85/15 Sn/Pb termination finish) must be considered as part of the program. In addition to standard PCB pad finish, lead free finishes including HASL will be included in the study. Wave soldering and intrusive soldering of plated though holes will be evaluated for features such as fillet formation, and solder quality. In addition, degradation to the board structure may occur due to extreme process conditions demanded by lead free soldering. A preliminary evaluation of conductively filled adhesives will be completed for micro-lead frame CSPs as part of the lead free development.

Flip Chip Assembly Issues

Flip Chip Reliability

More than anything else reliability concerns and the resulting need to underfill have significant impacts on almost all aspects of flip chip assembly. Process windows are largely limited by assembly defect and reliability issues. Unfortunately the most attractive designs and materials combinations, from a process and/or cost perspective, often do not offer the best reliability. Even for modest reliability applications process optimization therefore often requires a simultaneous optimization of the reliability within the given constraints.

Previous research has provided us with an in-depth understanding of the individual, competing, damage mechanisms contributing to failure under various combinations of processing, storage and service conditions. This year we have started on a carefully designed and controlled reliability test matrix aimed at identifying the best performing combinations of fluxes and encapsulants for two different contact pad metallurgies and three different substrate thicknesses. Of critical importance here is that the experiment take realistic manufacturing process variations to be expected into account. Considering combinations of 30-40 encapsulants and 10+ tacky fluxes is expected to eventually require the testing of upwards of 80,000 flip chip assemblies. We plan to continue, and hopefully complete, this project in the coming year.

In addition, we plan to conduct in-depth testing of the most promising materials combinations from the above matrix in terms of other materials (solder mask, passivation, laminate), design (layout, gap sizes), and loading mode (moisture exposure, aging, handling, thermal cycling parameters) variations.

Independently of this we plan to continue fundamental studies of individual damage mechanisms, notably encapsulant fillet cracking and delamination under the various loads. It is also likely to be necessary to continue ongoing studies of solder fatigue. Combinations of theoretical (modeling) and specifically designed experimental studies will be aimed at developing more appropriate accelerated tests and eventually extrapolating the test results to estimates of ‘life in service’. In terms of the latter we expect only to be able to make rather conservative estimates for specific cases within the next year but even this should have major consequences.

Similar studies are anticipated for other adhesives applications, notably heat spreader (lid) attach and perhaps optoelectronics packaging (see below).

Yield/Defect Prediction

Overall flip chip assembly yields are, of course, dependent on a very large number of factors as well as on the definition of a ‘defect’. We have, however, taken a step-by-step approach to this, identifying specific defect mechanisms and working to predict their consequences in a quantitative fashion. The aim is here (1) to identify the factors influencing the specific defect levels and (2) to develop tools to help in trade-off decisions and design, materials selection and process optimization.

The major problem in addressing any of this experimentally is the level of statistics involved. Process development efforts usually do not address defect levels below, say, 0.1% directly. This may make, for example, the definition of process windows a matter of quite uncertain extrapolation. We address this by (1) developing computer codes or algorithms to predict specific defect levels based on the (input) statistics of the underlying parameters, (2) specifically designed experiments to validate assumptions and calibrate the predictions.

So far, we have completed a substantial part of this for the defect mechanisms that are most sensitive to chip and substrate pad design, placement and collapse in reflow. We have documented case studies illustrating the use of the corresponding tools in design optimization. We do, however, plan significant improvements. This will include the incorporation of a growing data base of pad configurations and dimensions into the user friendly computer program, eliminating the need for separate numerical calculations of solder joint shapes. It will also include the experimental identification of important assumptions (input) for the placement yield prediction, such as ‘sticking’ or ‘slipping’ on the edges of mask and pad openings and the actual placement accuracy for real components (see below).

Another potential source of defects is fluxing. Depending on the choice of flux and fluxing method shorter, possibly damaged, solder bumps may not always reach sufficiently deep into the flux in time to ensure robust soldering. We plan to address this with individually measured, traceable bump heights to provide input to a fluxing defect prediction program to be developed as well. This should offer a powerful tool for the establishment of fluxing process windows.

Chip and Substrate Design Guide Lines and Specifications

The development and optimization of defect prediction software and, of even more importance, the assessment of necessary input and assumptions are ongoing activities (see above). ‘What if’ studies based on this have proven powerful in optimizing specific chip and substrate designs. However, effective optimization of chip/substrate pad layout and pad configurations also required the consideration of underfill process and reliability effects.

The generalization of all of this into general design guidelines is far from trivial. However, a step-by-step guide (‘cook-book’) to design optimization will be developed next year. Realistically achievable specifications in terms of substrate warpage and tolerances, as well as solder bump volume variations and damage, will also be recommended.

Flip Chip Assembly in Air

There is an overwhelming interest in avoiding cleaning under the flip chips, i.e. using no-clean fluxes. Because of flow behavior and influence on reliability only a rather small subset of these are actually acceptable for flip chip applications. In general, no-clean fluxes tend to have relatively low activity. They thus usually require nitrogen reflow to ensure good wetting and collapse of the solder joints to their equilibrium shapes. Good wetting promotes high soldering yields and sufficient bonding to (intermetallic formation with) the contact pads to survive thermal cycling. Depending on the specific substrate pad design a full collapse may be necessary to compensate for the combined effects of substrate warpage and ball height and pad size variations. Also, an incomplete collapse is likely to be less reproducible and thus leads to larger variations in gap size (standoff) between chip and substrate. This would lead to increased edge fillet height/thickness variations in an automated underfill process and thus significantly affect process development and assembly reliability.

It would, however, be attractive to eliminate the need for a nitrogen reflow ambient. In particular, current recommendations for eutectic Sn/Pb based 0201 assembly specifically involves air reflow. Integrated assemblies would thus seem to require flip chip reflow in air. Indeed, initial experiments have demonstrated flip chip assembly with no-clean tacky fluxes and air reflow. However, wetting and collapse was clearly reduced and so was the resulting thermal cycling resistance of the underfilled assemblies. Further work is therefore planned to identify a better flux and quantify optimized process windows, taking the above concerns into account. Alternatively, if a satisfactory flux cannot be found, the consequences for reliability and assembly yields will be quantified.

Fluxing Alternatives

Both liquid and tacky fluxes may be applied inside the placement machine. However, we have not found significant advantages to the dispense of a liquid flux in the machine. In general, liquid fluxes are distributed across the substrate (die site), not just located on the bumps or contact pads where they are needed. Reliability and, in particular, moisture resistance of the underfilled assembly is therefore usually reduced. Liquid fluxes also offer relatively little tack. In contrast, no-clean tacky fluxes which are reasonably compatible with preferred underfill materials, and thus offer better reliability, have been identified. However, dipping the solder balls into a thin film of a tacky flux inside the placement machine may slow down flip chip placement by up to 10-15%. It is therefore often attractive to apply the flux outside the placement machine.

Numerous new materials have become available since studies with liquid fluxes were last conducted. Also, Asymtek has promised us a so-called Flux Jet which effectively dispenses a much thinner, uniform layer of a liquid flux. A new effort to identify attractive combinations of underfill materials and liquid fluxes is therefore planned. Soldering and reliability will, of course, be assessed. Special attention will, however, be paid to the consequences of applying the flux to the substrate rather than to the solder balls. In the case of dipping, damaged solder balls that do not reach into the flux still tend to regain their original shape in reflow but they do not solder well to the substrate pads. With flux on the pads they would end up in contact with the flux remaining after the ‘soak’. Whether or not this is sufficient to ensure soldering remains to be tested. In general, the consequences of liquid flux application and flux thickness on expected assembly defect levels will need to be assessed. A user friendly computer program may well be needed for process optimization.

Reflow Encapsulants

An increasing number of materials have been developed that can be dispensed before chip placement, serving as fluxes during reflow and subsequently turning into an underfill layer. We have investigated almost all candidate materials so far. In case studies we have developed optimized processes for each, assessed their limitations and potential advantages. By now we have established an in-depth mechanistic understanding of the individual issues and process steps. We have started to determine generic limitations in terms of die size, as well as die and substrate layout. Not surprisingly, the approach proves quite sensitive to substrate dryness. Manufacturing relevant storage and bake out procedures still need to be established.

Next year we plan to continue to test new materials. We shall, however, emphasize the establishment of specific process windows and the formulation of a process ‘cook book’ along the same lines as for the regular underfill process.

Underfill Dispense Process

So far, we have produced a first 67 page manual outlining practical issues and suggestions for selecting dispense equipment and underfill materials, practicing with both, developing the actual process for any given product, and finally failure analysis (trouble shooting). Particular emphasis was placed on the establishment of a systematic database to allow for rapid, product specific process development and trouble shooting later on. The document will be updated considerably this year

We shall continue to conduct experiments on the fundamentals of dispensing and materials flow. The aim is to produce mechanistically based guidelines to speed up process development further, as well as offering better control and reproducibility, for any given application. Materials are being characterized in terms of automatic fillet formation and wetting, as well as reliability and compatibility with fluxes, solder masks, chip passivations, pad and solder metallurgies. Next year we plan to improve on the format of this, eventually computerizing it all, as well as adding considerably to data bases and generic guidelines. The final product will be a true step-by-step ‘cook book’ that can be used to train new underfill process engineers as well as supporting experienced people.

Transfer Molding

A potentially attractive concept in flip chip component (BGA, CSP) manufacturing is to simultaneously underfill and overmold the component, thus eliminating the need for a separate underfill step and significantly increasing throughput. Several groups are currently working on the development of transfer mold processes and appropriate materials for this purpose. So far, however, the simultaneous void free underfilling of 50-100 assemblies, as required in production, has apparently only been achieved on substrates with holes under the die. Considering the efforts usually expended in underfill process development to eliminate voiding this is not likely to be attractive for general use. Also, a systematic assessment of all potential aspects of reliability and damage is still required.

So far we have been working with Dexter and Neu Dynamics. Initial results suggest good reliability with a Dexter product, but more in-depth testing and failure analysis is required. In the coming year we plan to involve further collaborators and emphasize two issues: The testing of materials from other suppliers and the development of manufacturing relevant processes and/or equipment allowing the simultaneous molding of 50-100 assemblies without voiding under the chip. Special attention will be paid to effects of die size, die layout, standoff, and mold cap thickness on both process and reliability.

No-Pb FC Assembly

The use of no-Pb solder has unique consequences for flip chip applications. Because of the small dimensions involved reduced wetting and solder joint collapse may easily affect assembly yields. Together with a narrower reflow process window it may also lead to a broader gap size (standoff) distribution and thus problems for an automated underfill process. The need for a larger flux volume and/or activity reduces the process window and causes concerns with regards to underfill flow/voiding and subsequent reliability. The choice of contact pad metallurgy has been seen to seriously affect both intermetallic formation and ‘bulk’ solder composition after reflow. This has significant consequences for the solder joint fatigue resistance. Finally, the solder alloy may affect underfill delamination and, presumably, cracking in cycling quite strongly.

We plan to continue the establishment of assembly process windows. Notably, this will include the effects of reflow ambient, as assembly is likely to require lower oxygen levels than for Sn/Pb. In general, it will include assessment of effects of selfalignment and collapse on assembly yields, as well as the development of design guidelines for optimizing these. A particular concern is the possible dependence of solder joint properties on reflow profile and/or aging.

This will be addressed through detailed metallurgical studies and reliability testing. Our studies will be extended beyond the Sn/Ag/Cu/In, Sn/Ag/Cu, Sn/Ag/Bi, and Sn/Sb alloys to any other ones of potential interest for flip chip.

Assembly process windows will be established for the currently most popular alloy, Sn/Ag/Cu, and probably one or two more suggested by consortium members.

Flip Chip on Ceramics.

Over the years we have gathered considerable experience with regards to flip chip assembly onto conventional ceramic substrates. However, we have not conducted a systematic study along the lines typically employed within our consortium research. Notably, we need to look at some of the new high-CTE ceramic substrates. We plan to consider both HTCC and LTCC substrates.

We plan a limited effort to characterize ceramic substrates in terms of issues that affect assembly, i.e. the statistics of pad sizes and locations. Unlike for organic substrates random variations of these parameters within a given substrate may be significant. If they are, we plan to upgrade the existing placement yield prediction software to assess the consequences in a more user friendly fashion.

We obviously plan to address other issues of potential importance for assembly, including bump height statistics and fluxing. Indications are that both flux residues and moisture may affect underfill voiding quite differently than on typical organic substrates. The consequences for materials selection and process, notably bake out requirements, will be assessed.

No major reliability issues are anticipated, but we plan to conduct at least a few studies to check.

Flip Chip on Flex

Rigid flex applications do not always pose unique problems, but dynamic flex certainly do. This year we have designed dynamic flex test substrates as well as started identifying and contacting potential suppliers. We also conducted exploratory substrate characterizations, assembly and initial reliability studies on low cost substrates. Not surprisingly, fixturing for assembly proves to be an issue although obviously not an insurmountable one. Also, coverlay tolerances and adhesive bleed often lead to a need for contact pads to be very large. Various ways to deal with this are currently under investigation, and will continue to be so next year.

Solder spread and excessive collapse can be reduced by modifying the reflow ambient, but that does not seem attractive. Not surprisingly, attempts to do the same based on 'necking down' the traces leading to the pads have not shown much promise. Other approaches under investigation include the use of an appropriate no-Pb solder alloy, which might limit collapse to the part of the joint wetted, or identifying a reflow encapsulant which is viscous enough at reflow to prevent full collapse. Any approach that prevents collapse of solder joints to equilibrium shape has the potential for considerably larger variations in gap between chip and substrate. The statistics of this, and the consequences for assembly yields and an automated underfill dispense process, will be quantified.

Substrates with a regular photoimageable solder mask in the die region show promise, but the effect of single sided mask application on flex warp has to be addressed. Previous results show that balancing is an option but far from trivial. Cost will have to be assessed both for this approach and for nickel plating with selective gold coating in the intended pad area only.

Reliability issues include possible new effects of underfill properties now that this layer may provide the more critical mismatch. The sensitivity to moisture and aging, and the compatibility of underfill, flux, substrate material, solder and pad metallurgy, are expected to be unique to dynamic flex. The question to be addressed is to which extent thermal cycling resistance is still a concern at all and, if not, whether moisture and/or aging by itself is. Certainly, vibration and handling issues will be addressed, in particular the risk of damaging the brittle underfill edge fillets.

Experiments are also planned using Anisotropic Conductive Adhesive films (ACFs) on low cost dynamic flex. Obviously, this eliminates excessive collapse concerns and a less brittle material may actually offer better overall reliability than a typical underfill.

Optoelectronics Packaging

Like electronics packaging, optoelectronics packaging spans a broad range of dimensions and accuracy requirements. Optical alignment may require high or ultra-high accuracy depending on whether single or multimode fibers are involved. Components needed for long distance communication often require active alignment to accuracies well below 1µm, although this may be somewhat relaxed by the use of beam expanders and lensed fibers. Assembly then becomes exceedingly slow and the components very expensive, but profits in this area are tremendous. Automation is here primarily of interest because of the potential for reducing defects levels in an area where parts are scarce, as opposed to enhancing speed.

Extension of the same technology to more local communication and, eventually, to individual computers etc. will, however, require the kind of price drop, yields and volume capacity only achievable with higher speed automation. This can only be achieved through well coordinated efforts in terms of design, materials, process, and equipment development. Currently, many of the issues and details are considered highly proprietary by the practitioners, but we plan to pursue some issues of generic interest within the consortium

We have already initiated an effort to identify current practices and issues. This will eventually involve visiting equipment suppliers, perhaps materials and components suppliers, as well as anyone actually building things. Our experts on systems and equipment are being drawn upon for overall assessments of the state of the art, alternatives, and potential.

In simple terms optoelectronic component, or first level, assembly may be broken down into (1) assembly of the electronics in ways that differ only in some details from what we are used to, and (2) assembly of the optical or photonics parts. The former may, for example, involve flip chip assembly onto ceramic substrates. The latter often involves some extremely small parts, as well as requiring (often active) alignment.

‘Prototype’ Assembly

As an overall reference point, we plan to work towards building a generic model component, then assemble this into a corresponding ‘product’. This will involve laser attachment to a submount, attachment of submounts to a thermoelectric cooler, fiber alignment and fixing, component assembly, fiber handling and splicing, and so forth. Each step of the overall process should eventually inspire individual research projects in the same manner as our ongoing consortium work on area array assembly. Currently planned projects are outlined below.

Optical Fibers

A significant 2nd level packaging issue is fiber handling and management. Components are often not available with the optimum fiber length for a given application. The assembler is therefore left with handling and managing excess fiber. A common problem often not discovered until much later, and thus requiring extensive repair/replacement efforts, is fiber damage during handling. Such damage is caused by bending, squeezing, cleaving, polishing and/or thermal mismatches, etc. Importantly, it is often sensitive to temperature and moisture. We plan to consider options including fiber cutting and splicing, as well as improved equipment and fixturing. Anyway, component assembly often involves cleaving, and perhaps polishing, of fibers. Research in this area will include cleaving, polishing, and splicing of fibers, as well as studies of mechanical damage, both immediately obvious damage and gradual weakening or degradation.

Other fiber related issues include pigtailing, aligning, and ‘fixing’ (with UV adhesive and molding, soldering, or laser welding & hammering) the fibers. It may include butt joining with an optical adhesive. The concerns are similar to the above. In general, we will be testing fibers and fiber assemblies. Damage and failure analysis will provide the understanding needed for optimizations, specification of tolerances (in handling), and life prediction.

AuSn Soldering

Currently, component manufacturing usually involves AuSn soldering for laser attach, and often also for other components. This is done in order to minimize outgassing/contamination. SnPb solders are considered less attractive, among other because of their tendency to creep. In any case the soldering process obviously has to be flux less. The AuSn soldering is often conducted in a N_2(10%H_2) while holding down the die with an extremely low, controlled force. Current practitioners often prefer heating the die as well as the substrate. The feasibility of eliminating this requirement as well as performing the soldering in a less demanding atmosphere without significant increases in defect levels or unacceptably narrow process windows will be investigated. Anyway, AuSn is rather expensive for mass production. We therefore also plan to investigate potential alternatives.

Adhesives

A number of practioners also use adhesives within the components. The use of UV curable adhesives, rather than AuSn, is potentially attractive from equipment and cost perspectives. However, supposedly current materials are often not very dispensable and may only have a useful pot life on the order of an hour. In general, materials and process optimizations are needed to achieve manufacturing relevant (automated) well controlled dispensing of reproducible 1μg deposits, etc. Reliability testing is also a concern. We plan to work with the materials suppliers to identify optimum materials and/or facilitate materials improvements.

Hermeticity & Outgassing

Concerns with regards to hermeticity and outgassing may often be addressed by serious ‘overkill’. If so, a better quantification of the needs corresponding to various levels of service conditions should offer significant improvements in terms of process flow and yields, as well as general cost reduction. Long term in-depth studies are planned, aimed at a fundamental understanding of damage mechanisms and remedies, the development of proper accelerated tests and methods of life time prediction.

Robustness & Reliability

As in microelectronics, the most important response parameters in process development are yields, performance and reliability. Long term in-depth studies are planned, aimed at understanding the consequences of standards like Telcordia, as well as of actual manufacturing processes and service conditions.

For a beginning, both wave guides and layered structures, such as most subassemblies, may often warp considerably when unattached. Incremental cracking or delamination of the solder or adhesive used to fix them in position may therefore easily lead to misalignment. Certainly, it will affect thermal conduction. We plan to conduct model experiments to evaluate robustness, durability and reliability of candidate materials. Depending on the application envisioned this may require thermal cycling and/or aging, as well as handling.

Robustness and reliability are, however, sensitive to design and process parameters as well. A special concern is the anticipated shipment of die attached and wirebonded subassemblies back and forth between different manufacturing sites (often continents), once true volume manufacturers become involved. This certainly will require an assessment of the robustness and packaging requirements. In all cases special attention will be paid to effects of materials and process variability, as well as of design details.

Reports

As in the current Consortium we will continue to provide access to the reports and presentations generated via a secure Web page. Meetings will also be held on a frequent basis to allow us to focus on specific technical issues or general project status. The final report will be issued on CD-ROM and each company will receive fifty copies for internal distribution. As before we will encourage the involvement of suppliers as Participants limiting their access to knowledge generated on their products.

Time line

The Consortium activity shall begin on January 2, 2001 and will be complete on December 31, 2001.   Due to the continuous development activity in the subject technologies we will report on a continuous basis in “Focus” work group meetings and somewhat more formal “General “ meetings. The “Focus” group meetings will be held approximately every twelve weeks or whenever technical developments require discussion. The “General” meetings will be held two times per year.

Cost

Companies that participated in the 2000 Area Array Consortium will be charged a fee of $50,000.00 for the calendar year 2001. Companies that have not been Principals in the Area Array Consortium 2000 will be charged $75,000.00 for the first year. Subsequent years would be $50,000.00. This is designed to reflect the fact that a great deal of the basic knowledge development was supported by the current Consortium Principals and that there should be value attached to that knowledge for new Principals.