FLIP CHIP ON ORGANIC SUBSTRATES

Peter Borgesen
Universal Instruments Corporation
Binghamton, NY

ABSTRACT
The attachment of a flip chip of moderate size and pitch to an organic substrate has lost much of its mystique in recent years. A small but increasing number of companies, including several contract manufacturers, is establishing flip chip capabilities. This can, in fact, be done in a step by step fashion and with moderate investments in facilities, equipment and training. Still, since only the few can afford to simply remain conservative in today's market, implementation of the technology will require an ongoing optimization supported by a sizable R&D organization.

Overall cost, yields and reliability are sensitive to a multitude of materials, design and process parameters and their interactions. Assembly yields depend, among other, on design, placement accuracy, substrate pad and solder mask tolerances, ball height statistics, substrate warpage, and fluxing technique. Assembly reliability varies with encapsulant and flux type, chip passivation, solder joint number and distribution, solder mask surface morphology and chemistry, laminate chemistry, substrate rigidity and pad metallurgy, and various process parameters in a rather complex fashion. All of this is exacerbated by a trend towards larger die, finer pitches and smaller standoffs, as well as the continuous development of new, improved and/or alternative materials. Observed dependencies can, however, apparently be rationalized and generalized on the basis of an understanding of the underlying mechanisms.

INTRODUCTION
The attachment of flip chip to organic substrates, whether as Direct Chip Attach (DCA) or as part of component manufacturing, offers a series of potential advantages ranging from cost to performance and achievable I/O count and distribution. High I/O die may only be accommodated by an area array, the only questions being substrate (ceramic or organic) and interconnect (solder or conductive adhesive). Area arrays may also significantly shorten signal paths, as well as minimizing electromagnetic interference (EMI) which is a concern for RF applications. Furthermore, a reasonably even distribution of power across the die, rather than bussing in from the edge, may be important for high power applications. The minimization (elimination) of package levels may also make the attachment of relatively low-I/O flip chip cost effective. The latter in particular is here driving an increasing number of companies to implement the technology.

One attractive feature is that a company may implement flip chip capabilities in a step-by-step fashion as far as investments in facilities, equipment and training are concerned. For example, depending somewhat on the type of existing equipment a regular SMT assembly line might be upgraded to allow prototyping and low volume flip chip production for less than $500,000. Importantly, such an upgrade does not have to slow down or limit the equipment in use for regular SMT. The decision to go with flip chip in a specific application may therefore be made on a case-by-case basis. A contract manufacturer may, for example, establish prototyping and small-volume capabilities, deferring scale-up until a large-volume customer comes around. At the other end of the spectrum, of course, a complete high volume flip chip assembly line may cost $5-7M and occupy roughly 2,000 ft^2 [1].

The development of a flip chip process for a specific product may, however, require considerable insight and sound judgment. Materials or process changes that were not even recognized as such at the time have later been found to seriously affect product quality. Although we are starting to codify a considerable amount of data and understanding in various ways, the technology is not yet quite mature enough for anyone to write a general process 'cook book' without being dangerously naive, instantaneously outdated and/or impractical. So far, there is therefore no substitute for the ongoing support from a large R&D organization.

The following offers a brief overview of the technology and some of the issues with emphasis on effects of materials, design and process parameters. This is all based on practical experiences from individual customer applications, results of internal R&D efforts, and basic insights gained through Universal Instruments' research consortia. Emphasis is placed on flip chip attachment to organic substrates with eutectic SnPb solder joints. References are, however, made to high-Pb, no-Pb and conductive adhesive approaches.

ISSUES
The primary issues to be considered before implementing a specific flip chip process include design, dimensional tolerances, and materials selection. The latter is here strongly complicated by questions of compatibility.

Materials Compatibility
The interactions between all the different materials in the system are primarily of concern in terms of their effect on moisture resistance and reliability. An underfilled flip chip assembly is somewhat unique in that it constitutes an integrated multilayer system with the critical connections (joints) firmly embedded in one of the layers. Before, during

and after cure the underfill will react with, dissolve, or allow the diffusion of, moisture and numerous other chemicals from chip passivation, flux residue, solder mask, laminate, contact pads, etc. The resulting modifications of the local underfill properties may often be quite substantial. These modifications are more or less critical depending on the detailed stress distributions. This means that the best materials combination, and the sensitivity to the choice, may depend strongly on the assembly design (die and substrate thickness, heat sink attach) and the loading mode (thermal, mechanical, environmental) of concern. Also, the effect of, for example, solder mask and laminate on the underfill adhesion to the chip passivation often depends quite strongly on the standoff, i.e. problems that were not significant at larger standoff may suddenly become very important as solder joint pitch and height is reduced. In general, the identification of materials compatibility issues is an ongoing battle against the rapid developments in this technology.

Chip Layout

Far from all users have full control over the chip design. Those that do may, however, still have to weigh several different factors against each other. Signal path minimization and an optimized distribution of power and ground connections across the chip should often be compatible with an economical substrate routing. However, only relatively complex chips with several metal layers usually allow for contact pads near or directly over the devices. On simpler chips and memory devices, where the risk of 'soft errors' due to alpha emission from the solder may require larger keep-out distances, a fine pitch perimeter array may offer considerable silicon real estate savings. On the other hand, wafer bumping currently tends to become increasingly expensive and/or offer smaller bumps with more height variations (and thus less compensation for substrate warpage, slower underfilling and reduced reliability) at I/O pitches below 6-7 mil. Depending on the substrate technology and tolerances, maximization of the I/O pitch may also strongly enhance effective placement yields. Finally, moisture resistance and reliability may depend quite strongly on the solder joint layout and distances to die corners and edges.

Eventually, many commercial chips are likely to be offered in a dedicated flip chip design. At the moment, however, almost all such chips are initially laid out for wire bonding. This often involves single perimeter arrays with pitches down to 3-4 mil or less. One option is then the application of a redistribution layer and an additional passivation layer. While the semiconductor manufacturer might consider the necessary lithography coarse and relatively inexpensive, the establishment and maintenance of such capabilities at a packaging facility may be a serious cost factor. An alternative is to metallize and bump the fine pitch pads as received. Figure 1 shows an example of a 4 mil pitch flip chip with eutectic solder bumps. Depending on the consequences for the necessary board technology this may sometimes lead to significant savings if combined with a mask less Under Bump Metallization (UBM) process.

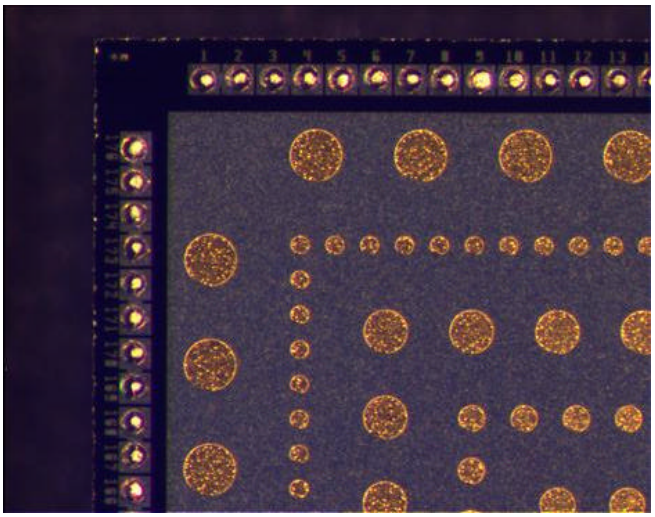

Figure 1. 4 mil Pitch Perimeter Array Flip Chip

UBM

Before soldering, the aluminum alloy contact pads on the chip must be coated with a solderable metallization. The requirements to this depend on the solder alloy, and on whether or not the solder is applied immediately afterwards. If, for example, wafers are stored and/or transported in air before solder application, oxidation is often a concern. UBM structures usually involve an adhesion layer, a diffusion barrier, a solderable metal and an oxidation barrier. A number of materials have been used on aluminum, including Cr/CuCr/Cu/Au, NiV/Cu, Ti/Cu, Ti/Cu/Au, and electroless Ni/Au.

While contamination (loss of solderability) is always a concern, none of the UBM structures appear to cause fundamental problems. The materials are, however, usually considered incompatible with semiconductor manufacturing, i.e. they must be applied after the wafer leaves the wafer fab. Most are applied by sputtering which, together with the necessary lithography, may add considerable cost. Savings might, in principle, be realized by using Pd which adheres directly to aluminum and may be deposited in the wafer fab. Unfortunately, Pd tends to embrittle SnPb solder joints to an unacceptable degree. Interestingly, this may not be so for some no-Pb solders.

So far, the only realistic mask less process appears to be the zincate based electroless nickel deposition. Like all such processes it is limited to deposition directly onto the exposed aluminum pads, some of which may be too small to support the solder joints without the simultaneous 'anchoring' on the passivation surface achieved by sputtered UBMs. Also, the stress exerted by the solder joints on the

underlying chip metallization structures during thermal excursions becomes correspondingly larger.

Chip Bumping

Depending, among other, upon the substrate and the final application wafers may be bumped with high lead, eutectic or no-Pb solder. Conductive adhesive based approaches may require adhesive bumps, electroless Ni/Au or Au stud bumps. Mean bump heights, bump height variations and bump damage have different consequences for assembly yields, process flow and reliability, depending on the approach. However, optimization usually involves maximizing the former and/or minimizing one or both of the latter two.

Solder bumping is now available as a commercial service from several sources at a reasonable price and, quite often, acceptable quality. Vapor deposition of high lead solder bumps has proven itself as a highly robust process. It is, however, usually very expensive, notably because of waste management issues. Also, the technique works less well for eutectic solder and shows little hope for most no-Pb alloys. Plating has been used down to very fine pitches (see Figure 1), but remains clearly experimental for most purposes at pitches much below 4 mil. This technique also shows little promise for most no-Pb alloys, in particular any with more than two elements. Moderately fine pitch wafers are quite readily bumped with electrically conductive adhesives, as well as with high lead, eutectic or no-Pb solders, using paste printing. Finally, solder bump transfer is showing considerable promise for pitches down to about 5 mil. Ni/Au and Au bumps may, of course, be deposited by plating or using a wire bonder.

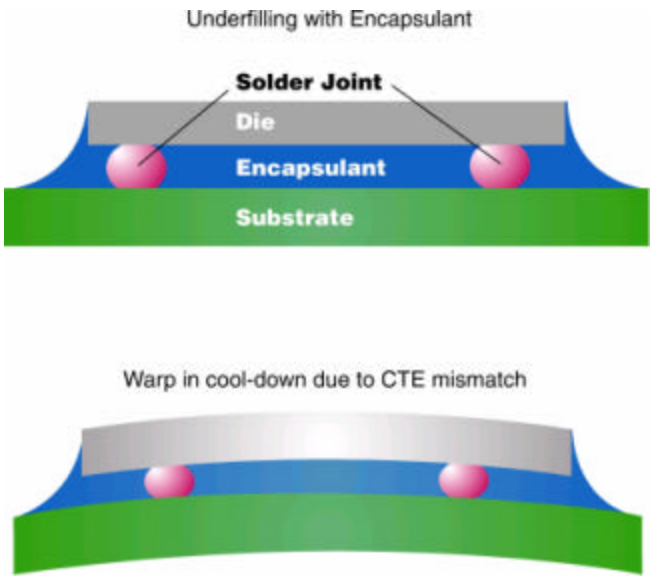

Figure 2. Encapsulated Flip Chip (Die) Assembly During Thermal Excursions

Dicing

Underfilling creates a rigid link between chip and substrate, usually leading to substantial assembly warpage during and after cool-down from encapsulant cure. (See Figure 2.) Subsequent handling or additional cooling in test or service may contribute further to the complex loads on the die. Depending on the rigidity of the overall assembly, dicing defects may thus become more critical than usual for other packaging approaches, leading to infant mortality and incipient failures.

Backlapping

Thinning of the die by backlapping obviously affects the assembly mechanics. The consequences for reliability, as well as for the risk of dicing defect induced cracking, depend strongly on the substrate. Backlapping has, however, also been seen to produce additional defects that may lead to die cracking during assembly, handling or thermal cycling.

Substrate Technology

In general, flip chip capabilities are strongly affected by the organic substrate technology and design. Pad metallurgy, as well as laminate and solder mask chemistries may strongly affect encapsulant adhesion. The layout, including whether or not vias are plugged and tented, may affect voiding and reliability in numerous ways. For high density substrates micro via imperfections and reliability may become an issue.

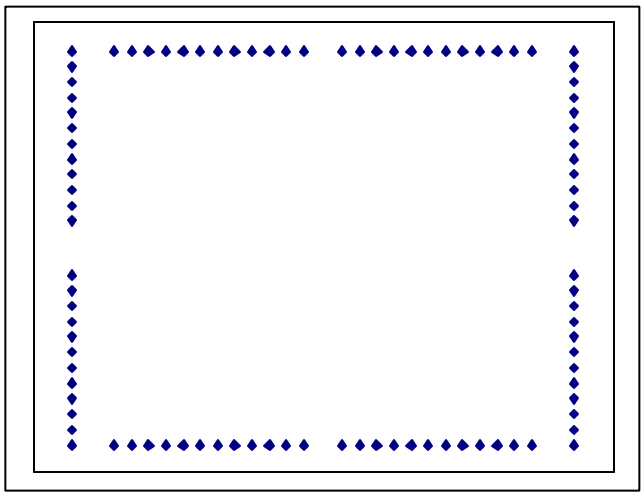

Figure 3. Foot Print of 8 mil Pitch Perimeter Array Chip

For conventional substrates commonly quoted tolerances of ±2 mil (at ±3σ) for line widths and solder mask openings, ±3 mil for mask registration, are usually quite realistic. The solder mask misregistration, in particular, leads to a requirement for relatively large mask openings. Figure 3 shows the foot print of a specific perimeter array chip. A reasonably robust substrate pad design involves lines

(traces) through solder mask traces along the perimeter. As illustrated in Figure 4, even a substantial solder mask shift still leaves exposed pads. Nevertheless, in the present case, the narrow trench opening has shifted too far (2.5 mil downwards in the figure) to accommodate the chip bump layout in Figure 3. On the other hand, the large trench widths required lead to a quite strong solder joint collapse. This rapidly becomes prohibitive for solder joint pitches below 8 mil. Finer pitches thus require considerably tighter mask tolerances or via-in-pad (no-mask) substrates, either of which involve additional cost. In contrast, conductive adhesive approaches, while placing higher demands on placement accuracy because of the absence of self alignment, allow the elimination of solder masks without such additional cost.

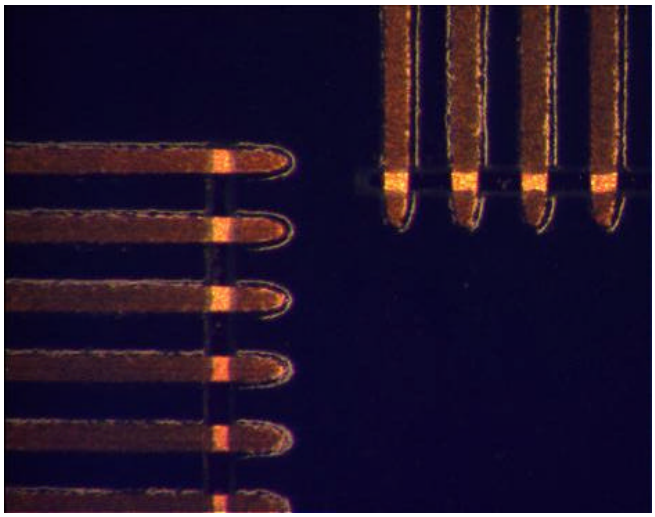

Figure 4. Substrate for the Chip in Figure 3 with (Nominally) 4 mil Wide Solder Mask Trenches.

High density substrate technologies are, of course, also limited by achievable via dimensions and via to capture pad registration. Some are also more prone to warpage in reflow. Furthermore, mask defined pads and built-up substrates allow for less solder collapse and thus less compensation for warpage and bump height variations.

Acceptable warpage levels and solder bump height statistics are mutually interdependent, as well as depending on solder alloy and whether or not the substrate is bumped too. The issues are again somewhat different for conductive adhesive approaches, but only the use of conductive adhesive bumps would appear to be relatively insensitive to bump height variations and substrate warpage.

Substrate Bumping

High-Pb die bumps require eutectic solder on the substrate pads, and some conductive adhesive bumps require adhesive paste. If the pitch is not too tight bumping may be relatively inexpensively achieved by stencil printing. However, placement of solder bumps directly in the wet paste led to increased bridging at pitches below 15 mil, i.e. finer pitches would require paste reflow, cleaning and coining of the substrate bumps before placement. The cost and effort of all this is not negligible and should be avoided when possible. Conductive adhesive bumps, on the other hand, allowed for placement in the wet paste at considerably finer pitches.

No-Pb and eutectic Sn-Pb bumps may not require separate bumping of the substrate pads. Still, the additional solder may help increase the die standoff. Substrate bumping may also help compensate for die bump height variations and substrate warpage. Coined bumps on the substrate may furthermore provide enlarged placement targets, compensating somewhat for pad and solder mask variations. Unfortunately, such large bumps are not realistic at the fine pitches (less than 8 mil, see below) where they would be most needed.

The ability of a given substrate bump height (or volume) distribution to effectively compensate for die bump height variations and substrate warpage obviously depends on the type of die bump. Eutectic die bump variations may, in fact, often be compensated for by a much broader substrate bump distribution. Non-collapsing high-Pb or adhesive bumps obviously require much tighter substrate bump distributions. In general, detailed statistical calculations are required to assess the effect of specific distributions on assembly yields.

Substrate Baking

Extraneous moisture in the substrate may affect this during reflow. More critically, it may interfere strongly with the cure and subsequent properties of the encapsulant. Baking to remove moisture before assembly or underfilling can, however, be avoided if the manufacturing sequence is properly planned and controlled. A necessary requirement is, of course, that the boards are received dry from the vendor.

Fluxes

The choice of flux requires considerable thought and judgment. The ideal flux has no residue, and thus does not negatively affect reliability and demonstrates high SIR values. Organic solvent cleaning is primarily applicable to ceramic substrates. For organic substrates the ultimate reliability is generally achieved with an optimized water soluble flux. However, the effort involved in subsequent cleaning under the chip, and the disastrous results of a slightly less than perfect cleaning, makes this unattractive. No-clean fluxes, on the other hand, invariably leave residues that may affect underfilling and reliability in complex ways. Flux selection here requires accounting for interactions with the encapsulant, solder mask, laminate, pad metallurgy and chip passivation, and the consequences for underfill flow, moisture sensitivity, and robustness in handling and thermal cycling. So far, commercially available liquid no-clean fluxes have not been seen to offer any obvious advantages when compared to pastes. Usually, careful testing allows the

identification of a tacky no-clean flux that flows well in the flux applicator, solders eutectic Sn-Pb flip chip joints well, and is reasonably compatible with all the other materials in the system. The same appears to be the case for at least some no-Pb alloys.

Reflow Encapsulants

A new development is the so-called flux encapsulants or reflow encapsulants. These unfilled materials are still somewhat immature, but some seem already applicable for specific environmental and reliability requirements. Obvious potential advantages include the elimination of a separate underfill step, notably the need for substrate heating during underfilling, as well as of the need for a nitrogen reflow ambient. Also, the absence of filler particles makes the filling of very small gaps relatively easy. Still, optimization of the dispense, placement and reflow process to ensure good assembly yields, minimize voiding and maximize moisture and thermal cycling resistance is far from trivial.

Fluxing

The dispensing of a liquid flux may take place in the placement machine, or in a separate dispenser just before this. In the latter case the volatility of such a flux may only allow a very short time interval before placement, but the time in the placement machine will be shorter.

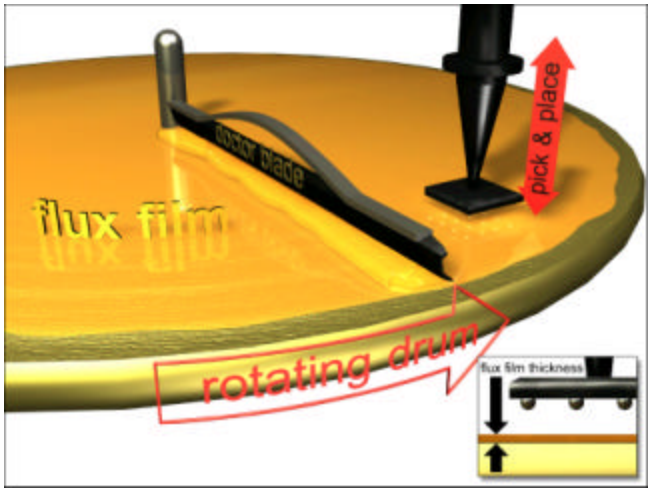

Figure 5. Typical Chip Fluxing on Drum Fluxer.

A paste flux may, in principle, be applied by stencil printing, but it may be difficult to limit the flux amount and resulting residue sufficiently. The preferred method is therefore for the placement machine to dip the chip bumps in a thin flux film on the way to placement. Figure 5 illustrates one way of accomplishing this, using a rotating drum and a doctor blade to maintain a specific flux film thickness. An optimized materials selection and control of the flux thickness to account for the chip bump height statistics has been found to provide for by far the most robust assembly process without compromising reliability and at a relatively low cost in terms of placement time.

Placement

Flip chip assembly generally requires a relatively high placement accuracy. The acceptable pick and place machine performance depends on the die design, substrate technology and attachment process.

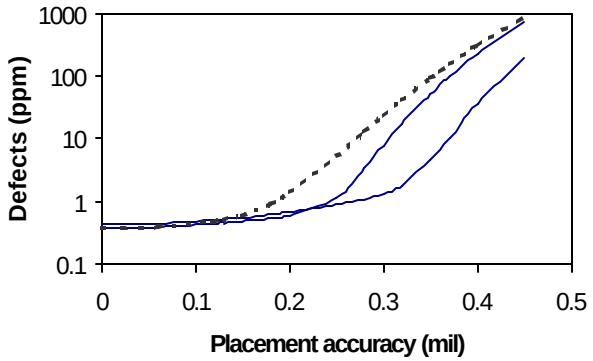

Figure 6. Placement related defects vs. placement accuracy (1 s) for typical substrate tolerances. 8 mil pitch perimeter array die placed on substrate with (nominally) 4 mil pads. Full curve: Substrate pads inspected to ensure minimum width of 2 mil.

A number of different machines offer a much better accuracy than the typical 2-3 mil (3σ) tolerances of conventional substrates (see above). However, the actual machine performance may still often affect placement yields quite strongly. Figure 6 shows the predicted effect of placement accuracy (1σ) on the defect level for the 8 mil pitch perimeter array die in Figure 3 placed on a conventional substrate with (nominally) 4 mil wide traces through solder mask trenches (Figure 4). These predictions were based on the assumption of typical pad size variations and a solder mask opening large enough to account for opening size variations and misregistration. Increases in the defect level to more than 1 ppm would thus be dominated by placement of the die bumps outside of the actual pad area (although still within the solder mask opening). The estimates should apply to most conductive adhesive approaches, to reflow encapsulant based assembly and, in spite of self alignment effects, at least conservatively to regular soldering. Optical inspection of the substrates, by the manufacturer, to ensure a minimum pad width of 2 mil would relax the requirements slightly but defect levels still increase rapidly for placement accuracies above 0.25 mil (one standard deviation).

Finer pitch die usually require alternative, high density substrate technologies, eliminating solder mask issues and often improving pad tolerances. However, a high placement accuracy is obviously still needed. At the extreme a conductive adhesive approach with 1 mil wide stud bumps and pads on a 2 mil pitch would require a placement accuracy of less than 3μm (1σ) even without bump and pad size variations.

The overall placement time clearly depends quite strongly on the machine, the substrate, the component mix, and general process optimization. However, any process with reflow encapsulant or adhesive cure outside the pick and place machine, perhaps even in the solder reflow oven, allows for a much greater throughput than achievable with, say, a chip bonder.

Reflow

Most no-clean fluxes, including any currently considered acceptable for flip chip assembly, require a nitrogen reflow atmosphere. However, even rather small eutectic Sn-Pb bumps, with the corresponding relatively thick oxide layers, do not require very low oxygen levels. No-Pb solder bumps are generally expected to require somewhat lower levels.

The only viable alternative to nitrogen so far seems to be the reflow encapsulants (see above) or conductive adhesives.

Contamination, Environment

Soldering is, of course, sensitive to contamination, particularly considering the fine dimensions involved. This is, however, by no means worse than what we are used to for wire bonding. An actual clean room is not necessarily required, but a clean environment is preferred.

More importantly, perhaps, both encapsulant properties and electrical performance of the assembly may be affected by flux residues, moisture, etc. Residues may be deposited in the reflow oven, because of prior contamination or outgassing of solder pastes and fluxes used in other parts of an integrated SMT assembly.

The question of moisture absorption before underfilling was already addressed above. Moisture exposure after underfilling, especially before curing, may also affect the encapsulant properties and perhaps assembly electrical performance.

Handling

Properly underfilled die are usually well protected from thermal mismatch induced stresses, but not necessarily from handling. In particular, vibration, bending or twisting of the assembly may damage the underfill, leading to faster delamination and/or moisture absorption.

Inspection

The choice of non-destructive in-line inspection techniques is very limited. Optical inspection offers only limited information. X-ray allow the ready detection of certain defects, most obviously bridging and completely missing solder bumps. Scanning Acoustic Microscopy reveals most underfill delamination and voids, and equipment is becoming available that may allow in-line use.

Underfilling

Along with the resulting difficulty/impossibility of subsequent repair the underfill process currently presents the greatest obstacle to a broader implementation of the Flip Chip On Board (FCOB) technology. New techniques under investigation include forced underfilling and vacuum assisted underfilling. In both cases, however, a major obstacle seems to be the development of manufacturing relevant equipment. An interesting new variation currently attempted by a number of groups is the simultaneous underfilling and overmolding with an appropriate compound. In principle, this should be achievable by simply modifying the gating in a regular molding process, but in reality somewhat different materials will be required.

As mentioned above, the use of a so-called reflow encapsulant would eliminate a number of current process difficulties, notably flow control and the consistent maintenance of a specific elevated substrate temperature to within a couple of degrees. The materials are, however, still in a rather early stage of development and testing. New concepts involving preapplication of the underfill at the wafer level, before dicing, offer even greater potential benefits but seem rather far from realization yet.

So far, the most common method of underfilling is clearly still by capillary flow. The development of a robust automated process for the rapid, defect free underfilling of millions of assemblies here poses quite a challenge. Even very small die, which may otherwise be underfilled by a single dispenser pass, usually require subsequent dispensing of optimized fillets along the ‘exit edges’. Optimization of the time interval(s) between passes must here account for variations in flow speed due to surface chemistry variations (incl. flux residue distributions), materials (flow) properties variations, temperature variations, and gap size variations. The gap between chip and solder mask may here vary with solder mask opening size and registration, as well as with pad width and solder bump volume. Encapsulant viscosities follow Arrhenius dependencies with activation energies up to 10 kcal/mole or more, leading to significant variations in flow speed for a couple of degrees increase or decrease in temperature.

The selection of dispense pattern and temperature may also depend on the tendency to form voids in the particular assembly in question. This phenomenon varies with encapsulant, flux, gap size, die passivation and solder mask chemistry, solder joint distribution and solder mask morphology, among other. Finally, the adhesion of some encapsulant types may depend on the flow temperature as well.

To make matters worse, data and trends observed in one particular assembly, or with a particular encapsulant, are often difficult to extrapolate. Although often modeled as regular liquids the heavily filled encapsulants may exhibit very different flow behaviors in some respects, depending on resin properties as well as particle sizes, shapes and concentration in complex fashions. Thus, for example, the flow speed dependence on temperature (activation energy) actually tends to vary with gap size and surface morphology.

Whatever the technique, the optimized underfill process should ensure void free underfilling, or the location of minimized voids in 'harmless' regions of the assembly, as well the formation of proper fillet shapes. The latter may, among other, be affected by variations in dispense volume and gap size under the die.

Underfill Materials

The selection of an underfill material does, of course, to some extent depend on the underfill method to be used. Notably, a forced underfill process might relax the demands on fluidity and allow the optimization of other materials properties, such as adhesion and moisture resistance. Even focussing specifically on underfilling by capillary flow, however, the material selection remains a critical and complex issue.

Different underfill materials exhibit very different capillary flow properties, in many respects deviating strongly from the behaviour of simple (unfilled) liquids. While all of them flow faster in larger gaps, some depend very strongly on the gap between chip and solder mask while others are almost insensitive to this. Some maintain very robust flow fronts, while others develop strong irregularities near obstacles such as solder joints, traces or solder mask features. Materials also exhibit very different sensitivities to aging in storage, in the machine and during the flow itself.

In addition, underfill materials vary strongly in terms of adhesion and moisture resistance. As mentioned above, this is further complicated by interactions with chip passivation, bump metallurgy, flux residues, solder masks, laminates, and contact pad metallurgies. Many of these interactions are furthermore likely to depend on assembly and design parameters such as standoff and rigidity.

Finally, many underfill vendors are relatively small operations. Materials reproducibility and availability has occasionally been a problem. The measurement of room temperature viscosity, as commonly used by the vendors to test for reproducibility and aging, has repeatedly been found not to reveal serious problems. It is therefore important to establish more realistic in-house tests for receiving-and-inspection. The issue of availability is best addressed by the identification of back-up suppliers.

'First time' selection of an underfill material should, of course, be made on the basis of the latest and best understanding of all these issues. No single material will perform the best under all circumstances, but lengthy in-house procedures in most companies usually do not allow the qualification of more than a couple of materials. It is thus recommended to identify a best 'overall performer' and a back-up material from a different supplier. A subsequent up-date of the materials selection is often only justifiable whenever the qualified one no longer 'does the job'. However, rapid changes in assembly design, economics and service (quality) requirements may make this happen soon enough anyway. At any rate, it is strongly recommended to maintain an ongoing effort in the area of underfill materials selection to prevent surprises.

Underfill Cure

Underfill materials may of course be under-cured. Indications are that some, at least, may also be over-cured, leaving an uncomfortably narrow process window for relatively fast curing materials. Under- and over-curing may affect the rate of delamination during thermal excursions as well as moisture uptake and diffusion. There is little doubt that the cure kinetics are affected by the small gap size, the proximity to chip and substrate, and perhaps the surface chemistries. It does not seem likely that these effects are all safely accounted for by DSC measurements on the bulk encapsulant. The definition of a process window is further complicated by the statistical nature of typical epoxy cross linking.

Typical cure processes may take anywhere up to 2 hours at 150-165C. This is not only slow but often hard on assembly components. Rapid (snap) cure materials often do not adhere as well. A new Variable Frequency Microwave technique allows curing of any encapsulant within a few minutes, apparently without any sacrifice in adhesion or moisture resistance. The robustness, convenience and possible side effects of this technique are, however, apparently still under investigation in various R&D facilities.

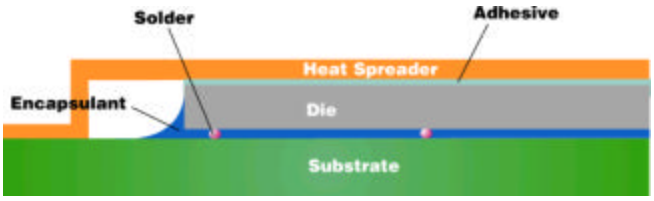

Figure 7. Flip Chip (Die) With Heat Spreader.

Heat Spreader

The use of lids, heat spreaders (see Figure 7) or heat sinks may affect the mechanics, and therefore the reliability, of the assembly quite dramatically. Notably, even with a completely compliant attachment/contact to the back of the chip anchoring to the surround substrate surface will tend to counteract the assembly warpage caused by the mismatch

between chip and substrate, thus changing the loads on the underfill. The selection of attachment method and material will usually depend on the required electrical and thermal performance. A careful mechanical analysis of the entire assembly is usually required for optimization and assessment of trade-offs between the thermal mismatch induced loads on the underfill interfaces and overall assembly warpage in subsequent second level assembly.

Reliability

Overall assembly reliability depends, among other, on encapsulant and flux type, chip passivation, solder joint number and distribution, solder mask surface morphology and chemistry, laminate chemistry, substrate rigidity & CTE and pad metallurgy, die thickness, standoff and various process parameters in a rather complex fashion. The relative importance of each individual factor obviously depends on type of loading (vibration, mechanical shock, thermal excursions, ...) but often also on the details of a particular type.

In general, assembly reliability is limited by the failure (open or short) of one or more solder joints. Solder extrusion and fatigue are, however, sensitive to the encapsulant as well as to properties of the solder joint. Extrusion and bridging depend on temperature, stresses and encapsulant void sizes and locations. Fatigue and catastrophic failure of a joint usually depend strongly on details of encapsulant delamination, although fatigue crack growth may occur without delamination as well. Delamination depends on underfill process parameters such as prebake, dispense temperature, fillet thickness, cure ambient and profile, as well as flux residues and subsequent moisture exposure. Worst of all, many of the above dependencies are interactive.

A major purpose of accelerated reliability testing of flip chip assemblies is to identify compatible materials and processes for the application considered. This is complicated by interactions such as those causing the preferred flux in a particular case to depend on substrate thickness. A variation in thermal cycling parameters often leads to a quite different relationship between encapsulant delamination and electrical failure. The extrapolation of observed lifetimes and/or relative trends to other (similar) assemblies and/or tests is therefore far from trivial. Luckily test results can, however, be rationalized and generalized on the basis of an understanding of the numerous underlying mechanisms. This helps reduce the assessment of design modifications and product changes to a significant but manageable task.

So far, the extrapolation of accelerated test results to life in service appears to be, at best, a matter of faith. A judicious choice of accelerated test parameters for a given case may, however, at least help ensure that we do not force false failures.

Repair

As far as the integration of DCA in a general SMT process is concerned, a major disadvantage so far has been the lack of repairability. Assemblies may of course be tested right after reflow. Although by no means trivial considering the dimensions involved, repairs may then be made before underfilling. This is, however, not the final and preferred stage.

Once the current thermoset encapsulants are cured, repair is no longer a realistic option. However, while still apparently not very robust, experimental repairable underfill materials are now reported to approach the reliability of most Chip Size Packages (CSPs). Further development in this direction could have tremendous consequences for the wider implementation of the technology.

Assembly Yields

Relevant assembly yields usually cannot be measured before commencement of manufacturing. Before then, however, process development frequently involves at least qualitative ('common sense') predictions. Important is often an assessment of potentially achievable manufacturing yields.

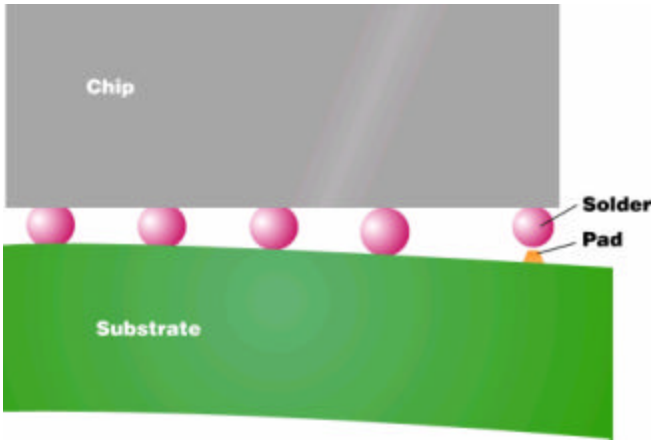

Figure 8. Typical Chip Placement on Substrate.

Potential assembly yields are strongly affected by substrate technology and design, i.e. whether contact pads are mask- or pad-defined, as well as pad size, thickness and shape. Aside from this, yields are largely determined by variations in solderability, bump heights and substrate warpage. Figure 8 shows an example where a combination of substrate warpage (in reflow) and an abnormally small bump in the most unfortunate location lead to an electrical open. Even a semi-quantitative assessment of the defect levels requires assumptions about the statistical parameter distributions to relatively far out on the tails. The necessary extrapolation of the experimentally measured distributions must be based on a mixture of sound judgment and an understanding of the mechanisms behind the variations. We have developed user friendly computer codes predicting the consequences of

variations in bump volumes, pad sizes and shapes, and substrate warpage across the die region and are currently investigating the nature of the individual distributions.

CONCLUSION

Flip chip capabilities may indeed be established in a step-by-step fashion without a major initial investment. However, flip chip process to organic substrates offers a variety of technical challenges in terms of final cost, process robustness (complexity), throughput, yield and reliability. Importantly, these issues are all strongly interdependent. Considerable insight and sound judgment is required, not just for initial implementation but on a day-to-day basis. Taken at face value new applications often appear to behave very differently from rather similar previous ones. Considering the common need for rapid product changes and process adaptation this presents a seemingly daunting challenge to design and process development. A sufficiently fundamental understanding has, however, by now been established to allow some codification and a general rationalization and extrapolation of test results. Still, a sizable R&D effort is required to keep abreast of new materials, design and process developments, as well as of totally new applications of the technology.

REFERENCES:

[1] Boulanger, Richard , Carbin, Jim and Viza, Dan, "Flip Chip Assembly: As Easy as 1, 2, 3," *Advanced Packaging*, Vol. 8, Number 3, pp. 28, March 1999.