Flip Chip Assembly Yield Prediction and Optimization

Peter Borgesen

Universal Instruments Corporation
Binghamton, NY 13902-0825
(607)779-7343
borgesen@uic.com

The attachment of flip chip onto organic substrates is gaining interest and acceptance for an ever increasing number of applications ranging from Direct Chip Attach (DCA) to component (BGA & CSP) manufacturing. In fact, it has been touted as the ultimate packaging technology, reducing the overall number of process steps and the materials consumption to an absolute minimum. Life is, however, usually not that simple. One reason for this is that the assembly process windows and the achievable assembly yields tend to become increasingly sensitive to variations in the small dimensions involved. Furthermore, the optimization and prediction of flip chip assembly yields is often particularly critical because of our (at best) very limited ability to repair.

Quantitative assembly yield predictions may, of course, serve as vital input for important cost assessments and decisions. In fact, many such decisions are indeed based on implicit yield predictions, often referred to as ‘common sense’ or ‘experience’, even if not recognized as such. Similarly, design and process optimization is often based on empirical extrapolations of rather limited and/or only partially applicable data. This can, at times, be dangerously misleading.

In general, flip chip assembly on organic substrates involves a series of steps, including fluxing, placement, reflow, underfilling and cure. Each of these, as well as contamination, may contribute to the overall defect level. Depending on our definition of a defect, we may also have to consider subsequent process steps such as lid attach/overmolding, ball attach, second level assembly and perhaps heat sink attach. Our current research efforts include assessments of the contributions of all of these. This presentation will, however, limit itself to a simpler definition of yields, based on the manufacturing of electrically functional flip chip assemblies on typical organic substrates.

It is commonly recognized that ‘alternative’ approaches such as conductive adhesives, reflow (flux) encapsulants and pre-applied underfill may require relatively high placement accuracies because of the lack of self-alignment. Also, some no-Pb solders offer less than perfect collapse and self-alignment. However, overly optimistic claims are often made for Sn-Pb solders because the effects of typical substrate tolerances, notably solder mask misregistration, on the effective ‘placement yields’ are ignored.

A user friendly Monte Carlo based computer program was developed and used for the assessment of effects of substrate design and tolerances on the assembly yields. An 8 mil pitch perimeter array chip with eutectic Sn-Pb bumps on a conventional FR-4 or BT type substrate of an optimized design still required a placement accuracy $\sigma_m < 0.25$ mil. Finer pitch chips require tighter solder mask tolerances, prohibitively large solder mask openings, or an alternative substrate technology. Unless pad size tolerances are also improved 4-6 mil pitch chips will require σ_m on the order of 3μm or less!

Contributions of fluxing to the defect level depend strongly on the fluxing technique. Both dipping in a paste flux and liquid flux dispense involve a sensitivity to flux and bump height variations, including damage. Knowing the minimum flux amount required on a bump to ensure proper wetting in reflow it is, in principle, straightforward to predict the defect level but quantifying the statistics of flux height variations is usually exceedingly difficult. The consequences of the negligible amount of tack offered by most liquids will be specific to the chip and assembly line in question. Still, guidelines for process optimization are readily developed.

Another potential source of defects is bridging or opens due to the combined effects of solder bump height variations, substrate pad size variations and substrate warpage in reflow. These effects depend, to some extent in contrasting fashions, on substrate technology and design, i.e. whether contact pads are mask- or pad-defined, as well as on pad size, thickness and shape.

A user friendly computer program was developed for the assessment of the effects of design and tolerances on the defect level. Intended for the use with BGA and CSP components as well, the program includes the effects of the statistical distributions of substrate and component warpages, substrate and component pad sizes, component bump heights or volumes, and solder paste deposits on the substrate. Addressing the effects of the statistics of such a large number of variables on assembly defect levels on the order of 1-100 ppm made a Monte Carlo approach unacceptably time consuming. A program based on an alternative approach was therefore carefully tested and documented. In its current form the program only addresses electrical opens, but an updated version will include the contribution of bridging as well.

Applied to chips with the tight eutectic solder bump height distributions achievable at moderate and large pitches, and a conventional substrate of optimized design, the program predicts a low defect level. However, this changes for finer pitches, alternative substrate technologies, some reflow encapsulants and some no-Pb solders.

For the sake of illustration, the program was applied to the chip in Figure 1. This chip has 998 I/O arranged in three rows around the perimeter and two rows across the center. The three rows are spaced by 6 mil and each has a pitch of 6 mil, center-to-center. The two rows each have a pitch of 12 mil. The solder bump height distribution had a mean of 3.5 mil and a standard deviation of 3%.

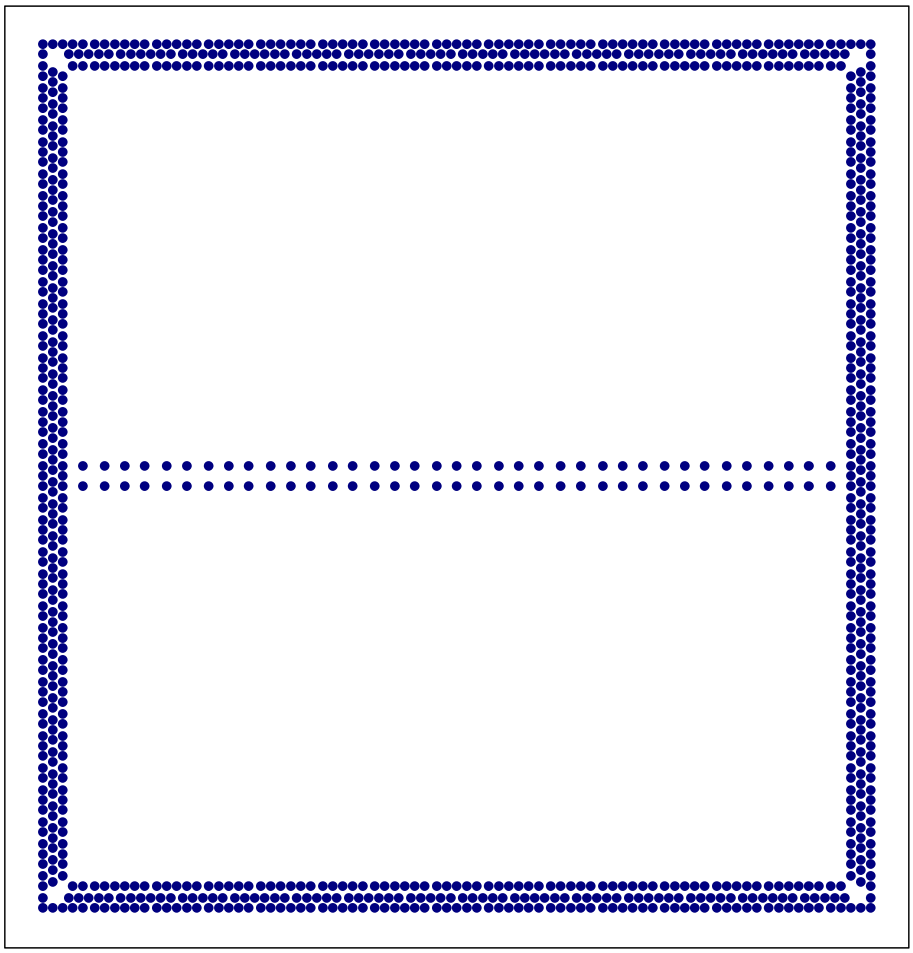

Figure 1: 0.5” square die, 998 I/O. Minimum pitch 6 mil.

Available (and affordable) substrate technologies allowed for two different designs, both based on via-in-pad. The mask-defined design involved 4 mil diameter solder mask openings over 5 mil diameter pads. The pad-defined design involved 0.5 mil thick, 3.5 mil diameter pads in larger solder mask openings. The predicted defect levels now depended on the pad and mask opening tolerances, as well as on the substrate warpage in reflow.

Assuming a quoted standard deviation of 0.25 mil in solder mask opening diameter and a substrate warpage of 0.3 mil across the die region in either direction, the mask-defined design would lead to about 20 ppm defects (electrical opens). Experience shows, however, that many high density substrates tend to warp more than that. A warpage of 0.5 mil would lead to 0.1% defects!

Assuming the same standard deviation for the pad sizes and a substrate warpage of 0.5 mil the ‘pad defined’ design should only give about 1 ppm defects, in spite of the smaller pad diameter. Interestingly, in spite of the much finer pitch this design only required a placement accuracy of σ_m=0.33 mil because of the tighter substrate tolerances.