

IMPLANTABLE MEDICAL ELECTRONICS ASSEMBLY – QUALITY AND RELIABILITY CONSIDERATIONS

Peter Borgesen
Universal Instruments Corporation
Binghamton, NY
borgesen@uic.com

Eric Cotts
Physics and Materials Science
Binghamton University
Binghamton, NY
ecotts@binghamton.edu

ABSTRACT

Implanted electronic devices face an unusually benign environment in many respects. However, mechanisms still exist by which an occasional device may degrade and fail in service. Because of the extreme financial and ethical liabilities often involved these warrant careful consideration in terms of how to test for them and, in particular, how to minimize the associated risk. We discuss long term degradation phenomena active in solder based assemblies at body temperature such as Kirkendall voiding and the growth of various intermetallics and whiskers. Depending on materials selection, supplier process control, and contamination these may lead to significant reductions in the resistance to mechanical loads common in service, or possibly even to failure in the absence of a significant load. Underfilling may reduce and/or eliminate the risk of most such failures but introduces alternate risks which must be minimized by optimized materials selection and substrate design.

Key words: packaging, reliability, pacemaker, medical implant.

INTRODUCTION

The total value of worldwide factory shipments for medical electronic equipment in 2002 was about \$50 billion. As one of the few sectors still only subject to off-shore outsourcing to a very limited degree, this typically high value – moderate volume one is seeing a rapidly growing interest by high-end US manufacturers. In recent years UIC's process laboratory has fielded requests for support on design, assembly, quality and reliability issues from manufacturers and would-be manufacturers of hearing aids, inhaler and insulin injector counters and

dosage controllers, CT-scanners, defibrillators and pacemakers. For reasons of quality and reliability requirements, more than anything, implantable devices here tend to stand out even in this rather tightly regulated field.

25 million Americans have implanted medical devices, but most of these (lens implants, heart stents, artificial knees and hips) have no electronics content. Still, implantable devices cover a growing range of products from sensors and drug delivery pumps to stimulating systems. By now, close to a million Americans have implanted pacemakers and cardiac defibrillators. Other stimulation systems are used to treat problems ranging from urinary incontinence to chronic pain, while deep brain stimulation is being used against diseases such as epilepsy, spastic tremor and Parkinson's Disease. While moderate in number, many of these are certain to gain wider spread use in the relatively near future. For example, only about 1% of the about 1.5 million Americans diagnosed with Parkinson's are considered candidates for one of the current deep brain stimulators, and only a fraction of these have had one implanted yet, but the price alone (about \$25,000 each) is certain to 'stimulate' new product development.

Even among implants, devices as directly critical to life and survival as pacemakers and defibrillators pose particular challenges in terms of quality and reliability. After all, even one early (unpredicted) failure may have extreme consequences, not only because of the potential loss of life but also because of the very high visibility of such occurrences. The electronics assembly parts of such devices are therefore invariably tested for effects of multiple solder reflow and repair cycles, cleaning (vigorous), storage conditions, and the various mechanical loads anticipated in handling and service.

Nevertheless, we argue that concerns remain as to the extreme statistics of failure, i.e. the risk of a rare defect driven early failure ('infant mortality') not eliminated by inspection or burn-in.

Systematic efforts to understand and quantitatively predict the long term reliability of microelectronics packages have traditionally emphasized effects of thermal excursions (cycling) and/or aggressive service ambients. While implantable devices often do undergo a number of thermal cycles (before implantation) this is, however, not necessarily our main concern. Rather, we are concerned with events not properly accounted for in accelerated testing of a finite number of devices, such as shorting through gradual whisker growth or solder extrusion, or opens due to Kirkendall voiding.

Also of concern are subtle long term degradations in mechanical robustness. Continued demands for better comfort, among other, require manufacturers to push the limit in terms of device weight, size and flexibility, while an unwillingness to accept life-style restrictions poses challenges in terms of robustness. Thus, devices must be designed to survive the high strain rates encountered by someone firing a rifle or being restrained by a seat belt in a car crash, as well as tested for both this and long term fatigue under more moderate mechanical loads. Depending on metallurgy, supplier and assembler process control, and contamination, the strength of maybe just a single bond may degrade over time in service to the point where device robustness suffers more than accounted for.

Taking a careful look at phenomena that will rarely pose a problem, we offer a brief review of some effects related, primarily, to solder based assembly of area array components. Emphasis is placed on Kirkendall voiding and two mechanisms specifically associated with Ni/Au coated contact pads. Accelerated test protocols are also discussed.

CONCERNS

Although cost is always an issue, even for high-end medical devices, this is not the primary reason why assembly yields are of concern. Rather, large defect rates invariably call for frequent repairs, perhaps even repeated repairs. In the case of solder attach, this involves localized heating and handling that may cause damage to neighboring components.

A much more insidious quality issue is, however, that of latent defects and damage. Joints or bonds may be marginal in a manner not detectable in even the most careful inspection, particularly when hidden inside or under a fine pitch area array component. The obvious response to this concern is a rigorous burn-in, but design of a proper procedure to eliminate defects without undue damage to surviving assemblies requires a detailed mechanistic understanding of failure mechanisms.

Overall, assemblies may be damaged in handling during and after manufacturing, as well as in service. Aggressive cleaning procedures are certain to weaken, for example, adhesive bonds and other organic layers. Also, implantable devices are obviously not subject to any significant thermal cycling in service, but they have to undergo multiple reflow and repair cycles, as well as see some thermal excursions in storage and transport.

The effects of all this on immediate, detectable, failure are here the lesser concern. Devices may even conceivably be briefly tested to ensure that they still survive more than the maximum design load and deformation before implantation. Mechanical wear-out (fatigue) effects pose a little more of a challenge. Still, it is comparatively straightforward to extrapolate results of accelerated isothermal testing to service conditions, and by incorporating various levels of 'preconditioning' damage in this testing processing and handling specifications can be established to ensure the necessary life in service.

More difficult to deal with are certain void growth and microstructural evolution effects which manifest themselves as reliability problems only in certain circumstances. These effects, such as Kirkendall void formation in Cu/PbSn solder joints, are generally present but minimally developed, such that they pose no threat to reliability. However, under certain circumstances, such as when manufacturing with poorly controlled metallization fabrication factors, these effects may be enhanced to the extent that an interconnect becomes too weak to survive realistic loads or deformations. Specifications on contamination or plating baths and processes are considerably harder to define and enforce (inspect or test for), at least until a sufficient mechanistic understanding has been established to allow the definition of accelerated test protocols and remedies. We shall address specific examples of this below.

MECHANISMS

In the following we shall be particularly concerned with mechanisms of degradation by which an electrical connection may become mechanically weakened. This will include Kirkendall voiding and the growth of intermetallic layers. The mechanical load on the actual bond to a contact pad in handling and service is limited by the overall assembly deformation imposed from the outside, and often by the flexibility or ductility of the wire bond or solder joint involved. As long as the bond strength exceeds this load limit, the actual value of the bond strength is not otherwise of concern. Whereas, the value of the bond strength quite abruptly becomes a problem once it degrades to below the load limit. Minimizing mechanical loads on the package will obviously extend the life in service. However, this alone may not allow us to ignore the potential degradation mechanisms as at least one of them may continue until the connection is severed, even in the absence of a load. In addition, we shall also briefly consider a couple of mechanisms that may lead to electrical shorts instead.

Kirkendall voiding

The vast majority of microelectronics packages are still based on wire bonding, usually Au wires to aluminum alloy pad surfaces. One of the most common long term degradation mechanisms in this case is Kirkendall voiding. This diffusion voiding effect follows an Arrhenius dependence and at body temperature a good bond should survive on the order of 10,000 years or more before weakening significantly. However, this voiding effect can be strongly enhanced by contamination of the bonding surface, as impurities are less soluble in the intermetallic phases and thus are 'swept' ahead of the diffusion front where they may precipitate and act as sinks for vacancies [1]. In addition, of course, any voids pre-existing at the interface can enhance the Kirkendall effect too. In either case, weakening may continue until a complete electrical open arises.

Kirkendall voiding may also become an issue in soldered assemblies, particularly whenever the most Sn rich intermetallic is highly rich in Sn so that its very open lattice allows for very fast diffusion of the non-Sn species. We would thus expect considerable Kirkendall voiding when soldering to Au, and indeed this is often observed although not always for that reason [2]. Figure 1 shows a whole array of Kirkendall voids along the interface between an Au stud bump and the first intermetallic layer, AuSn, formed (together with a AuSn₂ layer and AuSn₄ regions) by soldering with eutectic SnPb. However, although soldering to Au bumps is being considered for flip chip component assembly it is not a realistic candidate for implantable electronics, nor is any other configuration with thick gold under small solder joints. Thin gold layers are, on the other hand, a common means of protecting the solderability of, for example, nickel pads. Depending on the gold thickness this may lead to other concerns, as discussed below.



Figure 1. Kirkendall voids along interface between Au stud bump (top) and AuSn layer formed under AuSn₂ layer and AuSn₄ regions by soldering with eutectic SnPb.

The most common alternative to Ni/Au-coated pads is copper protected by either a thin organic layer (OSP) or preapplied SnPb solder, usually HASL. Soldering to copper the Kirkendall effect is not as pronounced as in the case of Au/PbSn interfaces, and voids between the

intermetallic layers are usually too small to be visible by optical microscopy [3, 4]. However, as Cu is still the faster diffuser through both the Cu₃Sn and the Cu₆Sn₅ layer on top, aging will lead to void formation at the Cu/Cu₃Sn interface [3-5] and/or the Cu₃Sn/Cu₆Sn₅ interface [5]. Normally, this growth is not even close to being a concern near body temperature, but as for the wire bonds prior contamination of the copper surface may strongly enhance this void growth if not properly removed. This should not be confused with the bubbles rising in liquid solder joints due, among other, to the evolution of volatiles in the fluxing reaction. A network of such voids might accumulate along the top (component) pad surface and facilitate subsequent fatigue crack growth there, but these voids may often not grow appreciably by solid state diffusion. For our present purposes, where thermal cycling is not an issue and mechanical cycling can be limited, we are primarily concerned with Kirkendall void growth enhanced by the 'Horsting effect' [1]. Under relatively rare circumstances this might be rapid enough to weaken the bond between the intermetallics, or perhaps even sever the joint completely, within a time of practical importance (service life). The way to eliminate this risk is to minimize pad surface contamination, among other means through appropriate fluxing. As far as accelerated testing for the phenomenon is concerned, we propose a protocol in the next section below.

The only mature alternatives to copper are the Ni/Au-coating approaches alluded to above. The thickness of the Au-films varies appreciably in these different approaches. There have been reports [6] that prolonged reaction between electroless Ni(P) and PbSn may also lead to the formation of Kirkendall voids near the Ni surface, but this appears to be an even less likely problem than for copper. A more complex mechanism is observed when the package includes a Cu-pad on the opposite side of the joint, and thus a ready supply of Cu to the solder. In this case, a build-up of a ternary (Cu,Ni)₆Sn₅ layer is observed on top of the Ni₃Sn₄ (which was formed on a nickel surface). Aging has here been seen to lead to void growth at the Ni₃Sn₄/(Cu,Ni)₆Sn₅ interface [7].

Electrolytic Ni/Au

As far as Ni/Au is concerned, our primary concerns are, however, quite different. First of all, the Au is plated onto the nickel surface to protect it from oxidation, but process variations may allow the nickel to oxidize beforehand or the gold to be porous and not sufficiently protective afterwards. A lack of process control may also leave an organic layer or other contamination on or in the gold. In either case soldering will be compromised, although a 'cold' joint may still be formed. Still, this should usually be detectable by even minor deformation of the assembly, i.e. mechanical screening or burn-in may be an option.

Just like for Kirkendall voiding, our *primary* concern is the formation of a solder joint that would be indistinguishable from a good one in initial mechanical tests but then degrade with time in service. Ohriner reported the formation of an AuSn₄ layer on a Ni surface [8], and Mei et al. associated the growth of such a layer to a certain thickness with the

premature failure of PBGA assemblies on electrolytically plated Ni/Au pads [9]. Zribi et al. explained this phenomenon by identifying the layer as the ternary (Au,Ni)Sn₄ phase [10]. Initial soldering leads to the complete dissolution of the gold layer and the well-known precipitation of AuSn₄ in the bulk of the solder joint. However, the ternary phase is thermodynamically more stable and therefore grows at the nickel surface, at the expense of the AuSn₄ precipitates, by solid state diffusion during subsequent aging. Figure 2 shows a cross section of a eutectic SnPb joint on electrolytic Ni/Au after aging for 40 hours at 150°C. The Ni₃Sn₄ layer has grown to a thickness of 0.4µm, while the (Ni,Au)Sn₄ is about 1.1µm thick. The (Ni,Au)Sn₄ growth was shown [11] to be controlled by Au diffusion through the solder rather than, say, the diffusion of Ni through the underlying Ni₃Sn₄ layer. The thickness was well represented by

$$X_{IM} = 9 * X_{Au} * (1 - \exp(-17.4Dt/d_m^2)) \quad (1)$$

where d_m is the largest distance of diffusion and D was calculated from an expression for the Au diffusion coefficient in Sn found in the literature [12], $D = 0.16 * \exp(-Q_{Au}/RT)$ with Q_{Au}=17.7kcal/mol.

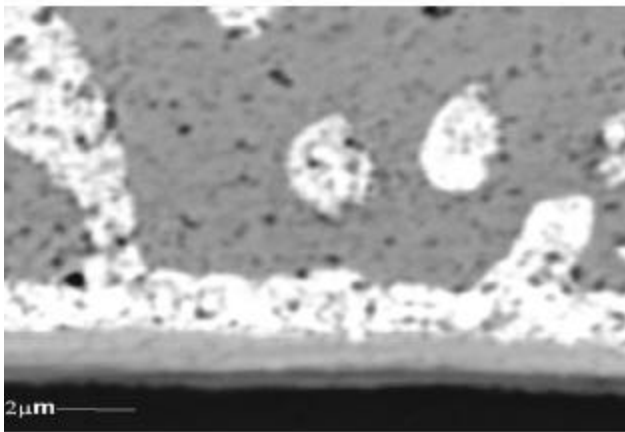


Figure 2. Cross section of eutectic SnPb soldered to electrolytic Ni/Au and aged for 40 hours at 150°C. Dark region at bottom – Ni. Next layer – 0.4µm thick Ni₃Sn₄. Lighter grey layer – 1.1µm (Ni,Au)Sn₄. White regions – Pb. Darker grey regions – Sn.

It has repeatedly been shown that Ni₃Sn₄/(Au,Ni)Sn₄ interfaces are mechanically unstable and their strengths decrease with increasing (Au,Ni)Sn₄ thickness, but as for Kirkendall voiding this is not of practical importance until the strength drops below the flow stress of the solder under the specific loading conditions of concern.

Figure 3 shows examples of load vs. displacement curves obtained for packages produced by reflowing 30 mil diameter solder balls onto 26 mil diameter Ni/Au pads and aging them at 125°C for various lengths of time.

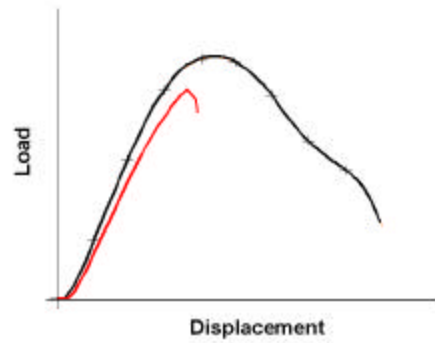


Figure 3. Load vs. displacement during shear testing of 30 mil SnPb balls soldered to 26 mil electrolytic Ni/Au pads and aged at 150°C. Higher maximum load and longer curve – after 250 hours. Lower load and abrupt drop – after 500 hours.

These packages were tested in shear according to the procedure described by Erich [13]. After about 500 hours of aging, the ultimate shear strength started to decrease and failure suddenly became much more abrupt. This was accompanied by a transition from ductile failure through the solder to brittle failure through the intermetallic layers on the contact pad. Figure 4 shows an example of this transition with a mixture of the two failure modes. Shear testing after aging at temperatures ranging from 100°C to 150°C showed the time for the interface strength to drop below the solder flow stress in a particular set of samples to vary as $\exp(Q_s/RT)$, where Q_s=19.2 kcal/mol [13, 14]. It is worth noting that Q_s agrees with the literature value for the activation energy for Au diffusion, Q_{Au}, above to within 8%, lending support to our interpretation. However, for several reasons, we caution against a simple extrapolation of our present results to ‘service conditions’.

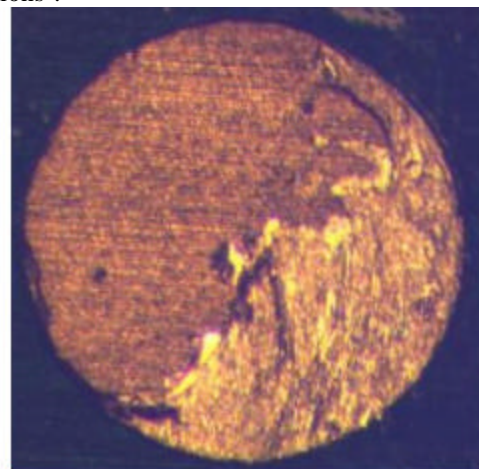


Figure 4. 26 mil diameter PCB pad after shearing off of SnPb solder ball. Top/left section shows exposed Ni₃Sn₄ intermetallic (brittle failure). Bottom/right part of pad covered with solder (ductile failure).

First of all, extrapolating our shear test results to 37°C (body temperature) we would predict a transition to 'brittle failure', or drop in shear strength, after 57 years or 33 years depending on which activation energy we assume (Q_s or Q_{Au}). However, our results correspond to a maximum diffusion distance, d_m , equal to the ball height in this experiment, 24 mil, whereas the collapse in assembly may be substantial and many area array components have smaller balls to start with. This is important because the time it takes to reach a certain intermetallic layer thickness X_{IM} , and thus for the interfacial strength to drop to any given level, is proportional to d_m^2 (Equation 1). In a CSP assembly the total solder joint height is often less than 10 mil, which would reduce the time to 'brittle' failure on the present Ni/Au pads from 33 to less than 6 years. In fact, with similar pads on both component and printed circuit board d_m would become *half* the joint height and the time would be reduced by another factor of 4 (X_{Au} would be the average of the original thicknesses on the two pads).

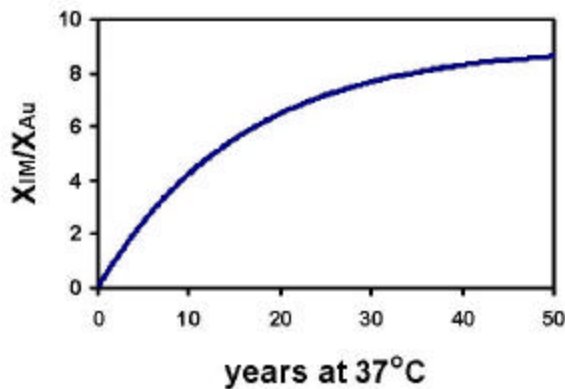


Figure 5. Ratio of (Ni,Au)Sn₄ intermetallic thickness to initial Au thickness on pad versus time at 37°C in 8 mil tall solder joint, according to Equation 1.

The present 'brittle' failure in shear is, as said, not necessarily a quantitative criterion for an actual device. On one hand contact pads may be designed for the interface to be less sensitive to shear, but on the other hand the intermetallic interface may be more sensitive to bending induced tensile loads. Most importantly, medical devices will almost certainly have been designed to prevent loads approaching the solder flow stress characteristic of our room temperature shear test. On the other hand, further aging is also likely to lead to further, substantial, weakening. Our shear tests above were conducted on pads with about 0.7µm thick Au, and Equation 1 suggests that 500 hours of aging at 125°C led to the build-up of a 1.3µm thick (Ni,Au)Sn₄ layer on the pad surface. While this was enough to cause 'brittle' failure, the equation also indicates that the final thickness after continued aging could be up to almost 5 times as high. Figure 5 shows the predicted ratio X_{IM}/X_{Au} as a function of time at 37°C for an assembly with an 8 mil standoff (only Ni/Au on component). A very large

fraction of the maximum achievable (Ni,Au)Sn₄ thickness would be reached within a 30-50 year life. The consequences for the strength remain to be quantified but they are likely to be tremendous for gold thicknesses like the present.

Realistic manufacturing tolerances do not allow for the control of electroplated Au thicknesses to much better (less) than 25-50 micro-inches (0.63-1.3µm). Depending on, among other things, the maximum load in service electrolytic Ni/Au coated pads may thus in fact present a concern. Immersion Au thicknesses, on the other hand, are certain to be much thinner but this technology leads to other concerns, one of them deceptively similar to the above weakening effect in appearance.

ENIG

Immersion Au is a self-passivating process commonly used to protect electroless nickel, and thicknesses are automatically limited to 3-8 micro-inches (0.075-0.20µm). The electroless nickel/immersion gold (ENIG) process is widely used in the electronics industry, for instance, in order to eliminate the space required for bussing in electrolytic plating. Immersion Au is a corrosive process that replaces each exposed Ni atom by two Au atoms and requires significant additions of something like phosphorous to the underlying nickel to prevent excessive corrosion. In fact, control of this appears to present an extremely serious concern.

Aside from the concerns shared with all Ni/Au coatings, a unique and widely recognized one is the so-called 'black pad' phenomenon. This is in fact a somewhat ubiquitous term which encompasses a number of phenomena related to failure at or near the Ni(P)/Ni₃Sn₄ interface. Most generally it refers to a lack of solderability of the Ni(P) surface due to a high amount of corrosion during the immersion Au process, but often the effects of various alloys or combinations of alloys near the interface are included as well.

One way or the other, 'black pad' usually refers to a 'time zero' phenomenon that may be detectable by even minor deformation of the assembly, i.e. in mechanical screening or burn-in. However an alternative mechanism by which a seemingly perfect solder joint may degrade over time may also be related to the corrosive 'black pad' effect. Confusing the research community for years, this mechanism leads to a measurable weakening and transition to an interfacial ('brittle') failure mode after aging in a manner virtually indistinguishable from that caused by the build-up of (Ni,Au)Sn₄ as discussed above.

Testing solder balls on ENIG surfaces from a large range of suppliers in shear after various periods of aging at 150°C, some showed a transition to brittle failure at the pad surface after 250-1000 hours. According to equation 1 a gold thickness of 6 micro-inches (0.15µm) or more might be enough to cause the build-up of more than 1.3µm of (Ni,Au)Sn₄ on the pad surface and thus such 'brittle' failure in our shear test. However, it should take much longer than this to do so with 24 mil tall solder balls, and careful analysis

showed no indication of such a layer. In fact, at least some of the Au was found to remain bound in $(\text{Ni,Au})\text{Sn}_4$ precipitates in the bulk of the solder and thus, unlike Au in AuSn_4 precipitates, not available for growth of a layer on the pad surface.

A number of studies have indicated correlations between the immersion Au induced corrosion, reflected among other in the appearance of Au 'spikes' into the Ni grain boundaries and thus an overall increase in the Au thickness as measured for example by XRF, and 'black pad' problems [15, 16]. One possibility is that excessive corrosion tends to leave too much crystalline Ni_3P , which isn't solderable, right underneath the Au. Importantly, however, we found numerous cases of good solder joint formation in spite of Au spikes. Since the corrosion rate drops strongly with increasing P content in the Ni [17] the black pad problem should as well. At the same time, however, too much P might lead to excessive Ni_3P as well. It is therefore not surprising if an apparent correlation with P concentration at the Ni(P) surface proves to be complex. While a concentration of less than 8-10% may be almost certain to give a problem, concentrations on the order of 15-16% seem to sometimes but not always be accompanied by problems as well.

Microstructural analysis of our shear test samples did not show a simple correlation between sensitivity to aging and the P concentration near the surface. Some samples with distinct Au spikes into the Ni grain boundaries failed in a brittle fashion after 250 hours of aging, but others still failed in a ductile fashion through the solder after 1000 hours. Extended growth of Ni_3Sn_4 during reflow and aging might well tend to leave only Ni_3P underneath, but there are indications that an $\text{Ni}_3\text{P}/\text{Ni}_3\text{Sn}_4$ interface may still be stable. As documented in a forthcoming publication, we find support for the suggestion that brittle failure is actually associated with the growth of an additional phase between the Ni_3P and the Ni_3Sn_4 .

Even if one does eventually succeed in identifying the phase which causes failure, we are still left with the question of which process, if any, presents the rate limiting factor and thus determines the temperature dependence. On the other hand, direct measurement of an activation energy for the transition to 'brittle' failure would require the availability of a significant number of similar samples. As might be expected from a phenomenon associated with the control and variability of a plating process the present problem tends to vary strongly from pad to pad, even within a single component site, and it remains to be ascertained whether a single activation energy applies for all pads that do exhibit the problem.

Whiskers

In 1986 the FDA advised that a group of pacemakers from a single manufacturer had been found to fail catastrophically due to tin whiskers growing from the tin-

plated case and shorting it to the crystal, and whiskers caused the failure of a commercial satellite in 1988. The growth of whiskers from pure Sn layers is thus a known concern in high reliability applications.

Long term storage (years) of plated Sn deposits at or slightly above room temperature has been seen to lead to the growth of up to 9 mm long single crystal whiskers. This occurs in the absence of ambient humidity and electrical fields and should not be confused with dendritic growth. Sensitive to a variety of parameters indications are that growth may be strongly enhanced by specific types of mechanical load. No single, widely accepted explanation has yet been established for this phenomenon, but an interpretation in terms of recrystallization [18] seems eminently reasonable. According to this the nucleation and growth of a whisker depends, among other, on the local combination of appropriately oriented high and low energy grain boundaries. Overall, it is expected that consistently preventing the growth of whiskers from a Sn coating would require the simultaneous control of so many factors that it may be impractical, if not impossible, in a manufacturing environment [18].

It is also not realistic to count on restrictions on the Sn layer thickness to limit the final length of whiskers. Whiskers of significant volume located in regions of no measurable thickness reduction are clear evidence of the very long distance diffusion involved. One of the few safe remedies may therefore be to eliminate pure Sn layers from the final assembly. Adding three percent (by weight) or more of Pb is commonly believed to prevent whisker formation, and the phenomenon is rare in SnPb solders. Occasional observations of 25-30 μm long 'whiskers' growing from a SnPb alloy may actually be hillocks formed by electromigration under high currents.

Recently there has, however, been a drive towards pure Sn plating of components such as ceramic capacitors or resistors as part of the transition of the microelectronics industry to lead free soldering. In addition, immersion Sn coating is under active consideration as a means of preserving the solderability of copper pads on organic carriers and printed circuit boards. In either case, the concern here is any coated surface left unsoldered. In addition, of course, it remains to ascertain which of the forthcoming lead free solders, if any, may be as resistant to whisker formation as SnPb.

Finally, indications are that conformal coating may reduce whisker growth, but it is not yet clear by how much or what would be the preferred thicknesses.

Underfilling

Defect free (void free) encapsulation in a hard material such as a conventional flip chip underfill may well suppress whisker growth sufficiently to prevent electrical shorts. It will certainly protect wire bonds and solder joints from mechanical loads and effectively eliminate risks of failure through reductions in the bond strength. Only complete failure by Kirkendall voiding alone would not be significantly affected by

underfilling, but this issue can generally be avoided with careful manufacturing practices.

Flip chips are normally underfilled (Figure 6) with a relatively rigid thermoset material in order to minimize solder joint fatigue in thermal excursions whereas a repairable, softer material is often used for BGAs and CSPs. The softer type of material tends not to enhance thermal cycling resistance, but that is not a major concern for implantable devices and a repairable material may even be used for flip chips. A softer underfill also tends to leave the overall assembly more flexible and often resists delamination under mechanical loads better, something which may be important as delamination will cause catastrophic failure once it reaches the first solder joint.

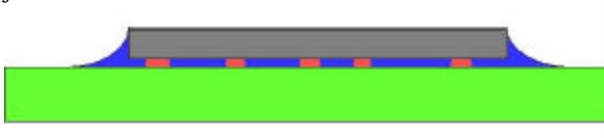


Figure 6. Underfilled flip chip assembly.

Another potential failure mechanism is however introduced by underfilling. Underfill flow and cure invariably leads to the occasional formation of small voids, and there is a particular tendency for some of these to become trapped between two closely spaced solder joints. The exposure of a sufficiently small area on the surface of an otherwise completely encapsulated joint tends to lower the effective melting point, because of capillary forces, as well as offering an effective relief for compressive stresses in the joint. Not only subsequent reflows, but also longer term storage at temperatures as low as 80°C have been reported to cause solder to extrude into such voids. Figure 7 shows an X-ray microscope image of a solder joint with an extrusion grown during thermal excursions.

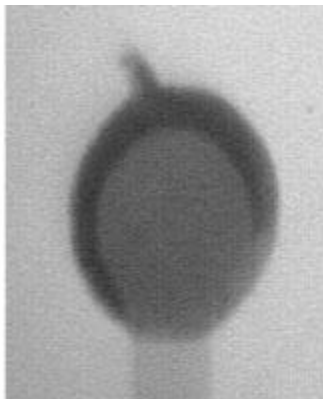


Figure 7. X-ray image of solder joint extruding into small void in underfill.

Extrusion into a void may reduce the resistance of the solder joint to thermal cycling but that is, as said, not a serious concern here. Bridging to a neighboring joint is of

course only really a risk at relatively fine pitches. Figure 8 shows an enhanced X-ray image of an 8 mil pitch flip chip with multiple shorts between the joints, while Figure 9 shows an 0.5mm pitch CSP assembly with up to 50µm long extrusions. It is not clear whether years at 37°C could ever cause the latter to grow much longer.

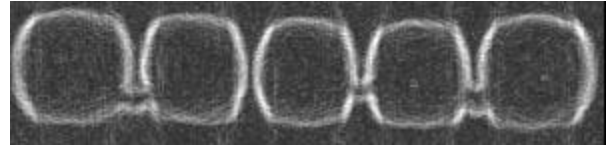


Figure 8. Enhanced X-ray image of solder joints in 8 mil pitch flip chip assembly extruding into voids in underfill and bridging to neighboring joints

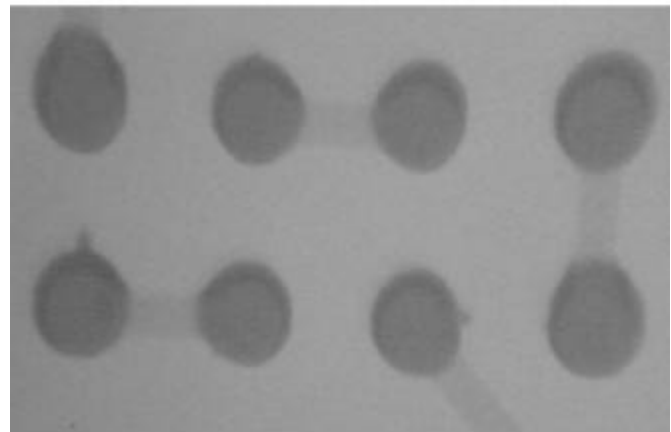


Figure 9. X-ray image of solder joints in 0.5mm pitch CSP assembly extruding into voids in underfill.

In fact, it is extremely difficult to quantitatively address the risk of bridging at the statistical level of concern. No two voids will expose quite the same solder joint surface area in quite the same location, so the occurrence and evolution of extrusions remains difficult to predict.

Finally, we emphasize that most underfills may degrade strongly under the aggressive cleaning in the manufacturing of medical implants. Materials selection will have to involve in-depth characterization of the effects of this on delamination, cracking and extrusion in repair and service.

‘REMEDIES’ & ACCELERATED TESTING

JEDEC has issued a document entitled “Tin Whisker Growth Tests” specifying two storage tests and thermal cycling, but the complex sensitivity of the phenomenon to a range of parameters make ‘acceleration factors’ of relevance to many years of service at best a matter yet to be researched in depth. Also, as mentioned above, the establishment of effective process windows is not entirely realistic.

The only realistic way of completely preventing problems with whiskers seems to be to avoid the use of pure and almost-pure Sn. Unfortunately, this may include at least some of the

currently favored lead free solder alloys. One way or another if whiskering is an issue underfilling should help. A hard underfill material is likely to provide the most effective whisker prevention, but hard underfills are usually not repairable and a truly soft material may reduce the risk and severity of solder extrusion into voids. On the other hand, matching the thermal expansion coefficient as closely as possible to that of the solder will also reduce the stresses causing extrusion, although mismatches with component and substrate prevent a truly stress free encapsulation. The finally preferred underfill may therefore be determined by other criteria, such as required flexibility.

One way to minimize the risk of extrusion and bridging is to use individual solder mask openings around the pads, rather than letting two or more share one opening. Underfill voids tend to form in the openings and rarely extend from one joint to another across a solder mask surface. Providing individual mask openings may simply be a matter of cost. The bridging in Figure 8 is all between solder joints within the same trench in the solder mask, a design made necessary by the rather poor tolerances of inexpensive printed circuit boards [19].

As for accelerated testing, the extrusion phenomenon does not seem sufficiently reproducible to allow the establishment of meaningful acceleration factors or the definition of test protocols. In addition, the underfill voids and cracks allowing for extrusion are often too fine to be detectable by inspection, even with an acoustic microscope. Underfilling, we therefore have to rely on a general optimization of the design, materials selection and process parameters.

As outlined above, our concerns with respect to bond strength degradation depend directly on the type and magnitude of mechanical loads anticipated on the actual product in service. These would have to be factored into the definition of specific test protocols. However, aside from that, the principles of test protocols should be straightforward.

Indications are that proper control of plating parameters (pH, chemistry, temperature, pad potentials,...) and ensuring a P content of around 10% may prevent 'black pad' effects. If not, an alternative to hypophosphite reducing agents might. However, it has yet to be firmly established that this is sufficient to prevent an occasional degradation of the intermetallic interfaces on the contact pads. In fact, considering the variability of the phenomenon, there isn't likely to be a realistic way to inspect or test for such problems. The only sure remedy would thus appear to be to avoid the use of ENIG in implantable medical devices. If there should still be a need for accelerated testing, a best guess might be that the phenomenon is somehow limited by the growth of the Ni_3Sn_4 layer, i.e. that test results can be extrapolated to

body temperature on the basis of an activation energy of about 14.6 kcal/mole [20].

Because of the inability to limit the Au thickness sufficiently and consistently, we also advise against the use of electrolytic Ni/Au pads for SnPb soldering. However, if electrolytic Ni/Au pads cannot be avoided, accelerated testing should involve the actual assembly configuration, as opposed to just solder balls, and the mechanical loading mode of concern. The safest approach is to drive the $(Ni,Au)Sn_4$ build-up on the contact pads to completion before testing, in which case no other thermal preconditioning is necessary. According to Equation 1, this can be achieved by aging the assembly for a time of about $d_m^2 * e^{8917/T}$ seconds at a temperature T (Kelvin), where d_m is the assembly standoff in units of cm. Alternatively, aging the actual joints for about 500 hours at 125°C or 120 hours at 150°C should be enough if preconditioning before testing includes all possible reflow and repair cycles as well. If you use larger balls for practicality of testing, or want to infer the reliability of assemblies with other gap sizes, aging time should be scaled as the square of the gap length dimension.

For the purposes of solder joint reliability, copper pads remain the most reliable, whether HASL coated or not. Wire bonding should be gold to gold. In either case the way to minimize the risks of significant Kirkendall voiding is to minimize contamination and, in the case of soldering, to ensure access of sufficient flux to the pad surfaces soldered to.

As for accelerated testing, wire bond results are commonly extrapolated to service conditions based on an acceleration factor of about 1eV per molecule (23 kcal/mole). The activation energy for Cu-Sn intermetallic growth is commonly expected to be around 1eV as well, or perhaps down to 0.7eV, but literature also quotes values of 0.5-0.75eV [21]. To be conservative, we might therefore recommend a value of 0.5eV (11.5 kcal/mole), so that 10 years at body temperature corresponds to 17 days at 150°C. In addition, preconditioning obviously needs to include all possible reflow and repair cycles.

CONCLUSION

The reliable packaging of medical implants requires a basic understanding and careful control of manufacturing processes. Long term degradation mechanisms exist which, if not properly controlled, can cause medical implants to fail through electrical opens or shorts. With careful consideration of the factors controlling device fabrication, these failure mechanisms can be reliably reduced such that they do not affect the life of the medical device.

Tin whisker growth has led to pacemaker failure but can probably be prevented under implant conditions by avoiding free surfaces of pure or near-pure Sn. Eutectic SnPb solder should not be a problem in this respect.

Another mechanism which may lead to failure even in the absence of a significant load is Kirkendall voiding in wire

bonds or solder joints on copper pads. These metallizations remain the recommended interconnect approaches from a reliability perspective, it is simply essential that careful control of all manufacturing steps be maintained.

There are distinct reliability problems with both electrolytic Ni/Au and electroless nickel/immersion gold metallizations, such that Cu metallizations are recommended whenever possible. The bond strength of eutectic SnPb solder joints to electrolytic Ni/Au coated pads is likely to drop significantly over several years in service, a weakening that would have to be carefully accounted for in the mechanical design of the device. Electroless nickel/immersion gold pads are subject to a complex degradation mechanism which, although not yet completely understood, is clearly sensitive to the control of the plating process in manufacturing. The variability of the effect from board to board, from location to location, and from feature to feature characteristic of a plating problem makes inspection and accelerated testing to a sufficient level of certainty virtually impossible. It is recommended that this metallization be avoided in critical implantable devices.

Underfilling of area array devices with a relatively flexible material should greatly reduce the risk of failure by long term degradation. However substrate design, materials selection and underfill process parameters should be optimized to minimize voiding, in particular between neighboring joints, and the risk of solder extrusion. The underfill must also be carefully tested for its compatibility with cleaning procedures.

Years of packaging research have yielded a set of assembly configurations which, when carefully and properly implemented, can serve medical electronics reliably. It is clear that the reliable packaging of medical implants requires a basic understanding and careful control of manufacturing processes. With careful consideration of the factors controlling device fabrication, reliable devices can be successfully produced.

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