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Step-by-Step Die Placement

Die placement techniques all have the handling of semiconductor devices in common. These techniques vary greatly, however, depending on the assembly process used. The most widely used assembly process involves attaching the die with silver-filled epoxy followed by wire bonding to the substrate. For most of these wire bond applications, the adhesive is dispensed directly on the placement machine. The die is then placed active-side up on the substrate and cured. This overall set of operations is typically referred to as the die placement process.

Other techniques have appeared recently in which the device is bumped and placed active-side down on the substrate. This technique, known as flip chip assembly, results in a quite different die placement process than the wire bond approach. In this article, die placement techniques for both wire bond and flip chip die attachment techniques will be reviewed. In each case, equipment and process characteristics will be presented and key machine and process issues discussed.

Introduction

The placement of semiconductor devices onto a substrate or a board is generally referred to in the industry as the die placement, die attach, or die bonding operation. Although the basic premise is the same, attaching the die to the substrate, the process, and the equipment configuration vary greatly. The variations depend on the application, the assembly itself, and, most of all, on the method used to interconnect the chip within the package.

The packaging for semiconductors must support four basic functions: power distribution, signal distribution, heat distribution, and environmental protection.[1] As the requirements for these functions evolve, so do the assembly processes. With today's trend towards increased functionality, as well as the ubiquitous "smaller, faster, cheaper" technology drivers, die assembly must perform several tasks. It must not only support the traditional mechanical functions, but also must minimize the overall assembly size, minimize electrical noise, permit maximum electrical performance, and ensure optimum heat dissipation.

The most widely used method of interconnection is wire bonding. In this method, a gold or aluminum wire is both bonded to the die circuitry and ball bonded to the substrate. This has served the industry well. Today more than 95% of all semiconductors are assembled using this technique. Another technique, however, is marked for future exponential growth. That is the flip chip interconnection approach. In this process, the bumped device is mounted to the substrate active side down. Since the active circuitry is facing down instead of up, as in the case of wire bonded devices, the technique is called "flip chip". Die placement processes, pertaining to both wire bond and flip chip interconnection techniques are discussed in this review.

General Die Placement Issues

In general terms, a die placement cycle consists of the following steps:

1. Pattern recognition of the substrate using global or local fiducials (or the circuit itself)
2. Picking of the die (either single or gang picking)
3. Imaging and theta correction
4. Placement of the die

Whatever die placement techniques are used, die presentation and substrate handling issues are shared by all. Dies may be presented for placement in various ways, such as in wafers, waffle packs, and tape & reel. Choosing the optimum die-feeding scheme depends on various factors, such as upstream processes, wafer yields, die sizes, and die sorting requirements. A wafer-handling scheme is well suited for applications where the wafer yield is high and the devices are small. On the other hand, tape & reel presentation may be appropriate for applications where the devices are larger and the wafer yield is low. In direct chip attach applications, for example, dies are sometimes processed prior to the die placement operation. In this case, the dies will have been sorted prior to the die bonding operation, and will be presented for placement via either waffle packs or tape & reel.

In the case of wafer processing, wafers are received after dicing on a film frame. Cassettes of 25 wafers are fed to the machine, and one wafer is indexed into the machine for placement. Frames are stretched to permit optimum mapping and picking. In order to pick a device from the frame, an ejector pin pushes the die off the frame while the pick head of the machine lifts the die.

Substrates vary widely in the industry. By far, most semiconductors today are bonded to metallic leadframes that subsequently become plastic packages such as TQFPs (Thin Quad Flat Packs). Other materials include rigid board materials, such as FR-4 and BT, ceramics, and polyimide flex circuits. Devices are sometimes placed in metal housings, as in the case of optoelectronic devices. Silicon itself may be the substrate in so-called silicon-on-silicon applications and other 3-D packaging schemes where dies are stacked.

The lighting scheme and camera resolution are critical and application specific. For flex circuit assembly, for example, blue lighting provides superior imaging resolution over the traditional 660nm red light. In the case of co-fired ceramics, the use of polarized light provides a better contrast between the alumina ceramic and the circuit metallurgy.

Die Placement and Wire Bonding

When placing a wire bonded device in a package, such as a TSOP (Thin Small Outline

Package), BGA (Ball Grid Array), or CSP (Chip Scale Package), the die is attached to the substrate by using an adhesive. Epoxy-based die attach materials are the most widely used. The organic adhesives are typically filled with silver filler particles in order to meet thermal and electrical conductivity requirements of the package. The silver-based adhesive may be screened or dispensed onto the substrate depending on the application. The amount of material required would vary with the die size. In general, the amount is controlled to preclude any material climbing onto the active side of the die, and to regulate the thickness of the adhesive otherwise known as the bond line.

The most common approach used for component assembly is to perform the dispensing and placement operations on one machine that is commonly referred to as a die bonder. For high volume, direct chip attach applications, such as Chip on Board (COB), Chip on Ceramic (COC), or Multi Chip Modules (MCMs), upstream dispensers or screeners followed by dedicated placement machines may provide optimum throughputs.

As we look towards the future, higher density wire bond packages are forecast for which the pitch between bond pads will be reduced to below 50 microns.[2] For such fine pitch applications, high placement accuracy is needed in order to precisely align the die and substrate bonding pads. Other novel packaging approaches, such as Chip Scale Packages (CSPs), also drive unique variants to the standard die placement process by adding heat and dwell times to the placement cycle.

Die Placement and Flip Chip

IBM introduced the flip chip process in 1964 when a new bumped die was used in the ceramic-based package called SLT. It has been used captively since then by companies such as IBM and Delphi Electronics. Merchant applications have emerged over the last five years as pin count, electrical performance, and miniaturization requirements have stressed the limits of the conventional wire bond process. Infrastructure issues, such as the cost and availability of wafer bumping and microvia substrates, are being resolved and 40-to-50% annual growth is projected.

The actual interconnection between a solder-bumped die and a given substrate is ensured by reflowing the die/substrate assembly through a nitrogen atmosphere oven. The temperature profile depends on the composition of the solder joint. The most common alloys are the high melting 95-97%Pb / 5-3%Sn and the lower melting eutectic alloy 63%Sn / 37%Pb. In such processes, there is no need for die attach materials. A fluxing operation, on the other hand, is required to remove the metallic oxides on the surface of the substrate, thereby ensuring good wetting. A typical flip chip line, including capacitor placement, is shown in *Figure 1 - Typical Flip Chip Line*.

Important die placement considerations include the die presentation and metrics (size, bump diameter, and pitch), material properties

Figure 1- Typical Flip Chip Line

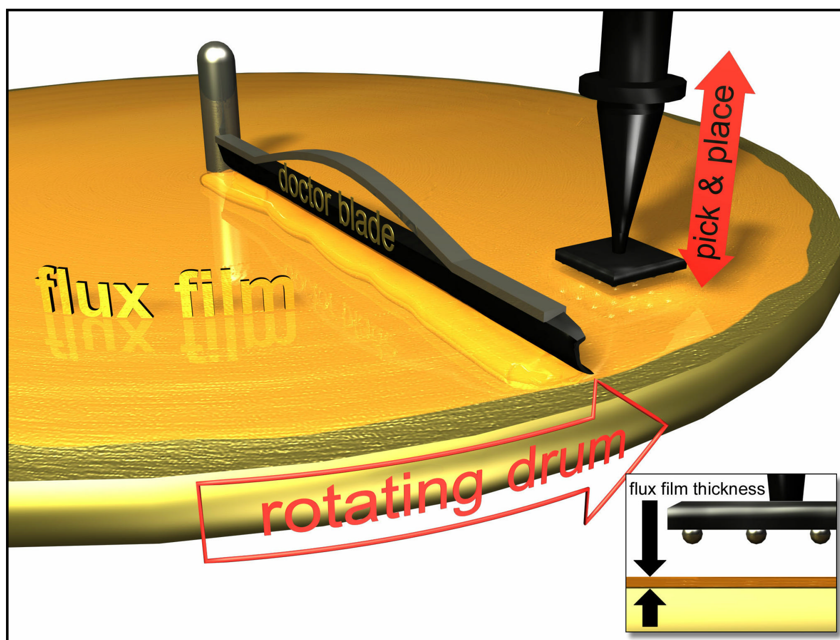

Figure 2- Rotary Thin Film Applicator

of the flux (viscosity, tackiness, wetting, and amount of residues after reflow), force of placement, and substrate imaging capabilities. The placement accuracy needed is dependent on the bump pitch and diameter. Because of the self-realignment properties of flip chip, tight pitch applications are possible. The semiconductor Industry Association (SIA) in its technology roadmap predicts that bump pitches below 100 microns will come of age in the second half of the next decade.[2] In order to place such fine pitch devices, high accuracy linear motor placement machines must be used coupled with high-resolution vision systems and high throughput capabilities.

There are several approaches to fluxing. The first approach is to dispense the flux, flood the chip site with the flux, and then place the chip down. A dipping method may also be used which is depicted in *Figure 2 - Rotary Thin Film Applicator*. It consists of dipping the die into a film of flux and then placing the chip onto the substrate. Introducing the low-solvent flux onto a rotating drum generates the film. Doctor blades ensure a uniform thickness. The film thickness requirements are dependent on the material properties, bump height, and the bump-to-bump height variation. The presence of post-reflow residues is of major concern because of the subsequent interaction with the underfill.

Even though flip chip has been in use for more than thirty years, it is considered an emerging technology. As such, new materials and processes are continuously being introduced into the marketplace. Underfill materials, for example, are being introduced that will combine the fluxing and underfill operation into one. Although limited in use because of reliability constraints, these flux encapsulant materials, as they are appropriately called, promise a significant cost improvement over existing underfill processes. Because these materials must be delivered prior to die placement, they will significantly change the flip chip placement operation.[3] Looking further into the future, wafer scale packaging promises to further simplify the assembly process by moving the underfill process to the wafer level. This will, however, create a whole new set of challenges to die placement.

Conclusion

Die placement operations are evolving as packaging requirements evolve. Processes such as fine pitch wire bond and flip chip assembly will drive a need for high-accuracy/high-throughput placement systems. Such systems will need high-resolution vision, flexibility in die feeding and substrate handling, and adaptability to evolving processes.

References

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