Assembly and Reliability of a Wafer Level CSP

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INTRODUCTION

Many of the CSPs in production today are presently being manufactured by the extension of the conventional package manufacturing techniques. Individual chips are attached to a base support substrate, such as a lead frame or a substrate, connecting the die pads to solder contacts used for the next level assembly. Electrical contacts between the chip and the carrier package can be made either by wire-bonding, tape automated bonding, or by flip-chip methods. A significant advantage of the chip-size package is that it can be made directly on the wafer, since each CSP covers only its individual chip site. Using this approach, each “package” is assembled to the corresponding IC while still on the wafer. The ICs can be burned-in and tested before being diced into individual, fully furnished packages. The definition of a true wafer-level packaging solution has been expanded to include packages that:

- use material and equipment that process die simultaneously on the wafer;
- are not dependent on layer fabrication off-line, or individual placement and connection of features;
- use equipment and processes consistent with standard semi-conductor processing;
- allow for wafer-level burn-in and test strategies.

Other advantages include:

- elimination of different redistribution and stack-up layers by a single layer of polyimide or any other dielectric;
- the process is independent of the fabrication of layers off-line, such as flex films, or the individual placement and connection of features;
- the process steps assure quick turn-over for new designs, as well as the ability to rapidly adapt to changes, such as die shrinkage [Juskey, 1998];
- wafer-level packaging eliminates risks of supply issues with a flex film, and the attendant inventory and scrap costs that this incurs during design changes or a product’s end of life [Elenius, 1999];
- in comparison to flip chip packages, the wafer-level CSPs provide equivalent size and performance, while retaining the advantages of an SMT package [DiStefano, 1997].

Currently, there are more than a dozen wafer-level CSPs available in the market. Some of the well-known ones include Flip Chip Technology’s Ultra CSP™, National Semiconductor’s MicroSMD, Fujitsu’s Super CSP, ShellCase’s Shell CSP, Amkor Anam’s wsCSP™, Tessera’s Wafer level μBGA, Mitsubishi Electric’s Molded CSP, and Sandia National Laboratories’s Mini BGA.

RELIABILITY OF WAFER-CSPS

The reliability of the wafer-level CSP is dependent on the structure of the package. Compared to conventional CSPs, the wafer-level CSPs have fewer problems such as pop-corning, die-substrate de-lamination, and other moisture-induced defects. The failure mode in CSPs during accelerated thermal cycling is affected by the construction of the package and the temperature extremes. The package can fail internally (within the package such as wire-bond, redistribution traces, tapes, leads, etc.) or due to solder fatigue.

The reliability data available in the industry is highly confusing. [Gaffarian, 1999], reports that wafer-level assemblies often show very few cycles to failure, and most of them require underfilling to achieve reliability comparable to conventional mounted packages. Reliability data on the Sandia MiniBGA™ package for the 0 to 100°C thermal cycle regime was found to be > 2000 cycles with underfill and less than 40 cycles without underfilling [Chanchani, et al., 1997]. Test results indicated (>1000 cycles) solder joint reliability of the Amkor Anam wsCSP™ format [www.amkor.com]. The μSMD from National Semiconductor Devices is reported to have passed 2300 cycles at the 0 to 100°C thermal cycles [Nguyen, et al., 1998].

The Tessera wafer-level μBGA package is built on multi-layer polyimide flex, supported by a layer of compliant encapsulation. The wiring layers are connected to the pads on
the chip by flexible bond ribbons embedded in the compliant material [DeStefanio, 1997]. Reliability is claimed to be high because of the flexible ribbon bonds that allow thermal expansion without damaging the solder attachment to the board. A number of results have shown that the μBGA package fails at a very low number of cycles, with the failures most likely occurring at the bonding pad [Wang, et al. 1998].

The package that has been used for our evaluation – Package A is different from other conventional CSPs in that Package A does not employ an interposer between the IC and the solder ball array. The assembly of the device to the board requires the assembler to follow specific rules to achieve optimal reliability, because the stress is taken up within the solder interconnection itself [Barrett, et al., 1998]. Since the intermediate substrate is absent in most of the wafer-level CSPs, the CTE of the package is significantly less than molded devices. Wafer-level CSPs combined with low standoff offer an unfavorable combination with respect to thermal reliability [Partridge, 1999].

Board level reliability of similar wafer level CSPs has been evaluated and published. Thermal cycle reliability testing of these packages has shown the ability to pass > 1000 cycles of 0 to 100°C and > 500 cycles for the –40 to +125°C. In all the cases, the failure mode of the package joints has been solder joint fatigue [Barrett, et al., 1998].

**PACKAGE A - DESCRIPTION**

The daisy chained parts (Package A) used for the assembly experiments do not have an interposer nor does it require underfill. The pads are routed to JEDEC standard pitches using CSP-size balls on the re-routed pads. This device is ideally meant for memory devices such as flash memory, DRAM, EEPROM, SRAM, and integrated passives in a variety of applications.

Package A is a true wafer level package as it uses standard semiconductor processing equipment to produce a thin-film redistribution layer and a wafer-level ball attach technology. The package uses a two-layer polymer dielectric system of Benzocyclobutene (BCB) and a thin film solderable redistribution layer of Al/NiV/Cu. The use of the thin film allows the use of a single metal layer for both the redistribution trace as well as the under bump metallization. BCB was chosen because it is compatible with copper metallization and has excellent resistance to moisture and chemicals [Elenius, 1999]. The total thin film thickness is approximately 10 microns. The thin-film redistribution layer construction consists of the following [www.flipchip.com]:

- Dielectric layer 1 for passivation and planarization of the die passivation (when redistribution is required);
- Al/NiV/Cu, a thin-film layer that is sputtered and then etched to form the trace and UBM pad;
- Dielectric layer 2 for passivation of the redistribution wiring and definition of the solderable area for the ball.

A standard ball attach process of fluxing, ball placement, and reflow is used for attaching the solder balls. Because the I/O pitches are standard, the only design limits with Package A are size of the die and the number of I/Os, for a larger die with big I/O there is a limit to the number of rows that can be redistributed. In cases of higher I/O count chips, it is often more cost effective to use a standard flip chip device [Elenius, 1999]. Thus, the package is a transition package between a CSP and flip chip.

Package A has 46 solder bumps distributed in an area array (6 by 8 pattern), depopulated at the center. The package is rectangular in shape with physical dimensions of 317*246 mils and a thickness of 43.8 mils (from the top of the die to tip of the bump). The silicon has an overall thickness of 27 mils and is attached to a flex layer with a thickness of 0.3 mils. The solder bumps have a mean diameter of 21.5 mils and a height of 16.5 mils. The package construction details are shown in Figure 1.

**TEST PLAN**

The main objective of the experiment were:

- To investigate and study the assembly issues concerning the wafer level CSP, Package A;
- To study the effect of using solder paste and flux on solder joint reliability;
- Assemble Package A on via-in-pad land patterns and compare the solder joint integrity on the via-in-pad connections with conventional NSMD pad connections;
- To study the effect of varying pad diameters on the solder joint strength for both the conventional and the via-in-pad structures.

A total of 96 packages were assembled on the test board. Of these, half were built using flux and the other half with solder paste. Nitrogen was used as the reflow atmosphere as it increases the wettability and reduces the chances of voids in the solder joint [Primavera, 1998]. For comparison, Package A was built on conventional Non Solder Mask Defined
(NSMD) pads and the via-in-pad design pads having NSMD geometry (Figure 2). Both the via-in-pad and the conventional pads had three levels of pad diameters available: 11 mils, 13 mils and 15 mils. Prior to assembly, the boards were characterized and documented. Table 1 shows the design values of pads and vias for the different sites assembled.

![Figure 2: Via-in-Pad and Conventional Pad](image)

**Solder Paste**

No-clean, Type IV, eutectic solder paste with a 90% metal content was used. Prior to use, the solder paste jars were kept in a running water bath at around 25℃ for 4 hours. The paste was then thinned by stirring it using a spatula. The paste bead diameter on the stencil was maintained at approximately one-inch.

**Flux**

Flux was applied to components before placement using the Thin Film Applicator (TFA). The TFA device is attached to the placement machine and is used to apply small and repeatable amounts of flux to solder balls on components. It has a rotating drum which has a flat top, coated with a thin, uniform film of flux. A fixed blade (doctor blade) maintained the thickness of the flux film. Before placement, the component was placed onto the drum surface by the pick and place machine, causing flux to transfer to the solder balls. The machine waits for 150 milliseconds before picking the component off the film and placing it onto the PCB. The thickness of the flux film applied was maintained at 4.5 mils.

**ASSEMBLY**

The assembly process was done in two parts; the first involved the assembly of packages using solder paste while the latter half was done using flux. The assembly process involved the following process steps:

- **Board cleaning** - Solder paste printing / fluxing - Print inspection - Component placement - Reflow - Electrical circuit test - X-ray inspection.

Prior to assembly, all the boards were visually examined to observe any defects such as debris, fingerprints, contamination, etc. The components assembled were baked at 125℃ for about 12 hours prior to assembly to drive away any moisture that could lead to defects. Representative packages were examined using x-ray for voids or any other defects.

A fully automatic stencil printer was used for printing solder paste onto the boards. Polyurethane, 9" long squeegees with a durometer of 95 on the Shore A scale were used for the printing operation. The squeegee angle was maintained at 60°.

A 5-mil thick, laser cut, stainless steel stencil was used for the printing operation. The stencil was characterized in terms of its aperture size openings. Before the solder paste was deposited onto the experimental boards, it was thawed and kneaded to attain a homogenous mixture with uniform viscosity. A few set-up boards were first printed in both directions in order to stabilize the process. After attaining the required print quality, the experimental boards were printed. Visual inspection with an optical microscope was used to determine the quality of the print deposits. Print parameters used for the build are:

- **Print Pressure** – 0.49 kg/linear inch;
- **Print Speed** – 15 mm/sec;
- **Print Gap** – On contact;
- **Separation Speed** - 0.3 mm/sec;
- **Strokes** – 1;
- **Stencil Wipe** – 3 prints;
- **Squeegees** – Polyurethane 9 inches - 95 durometer;

A flexible and highly accurate placement machine was used for placing the components on the board. The components were picked from matrix tray feeders and placement and reflow were performed using an inline board handling system. The same program, with minor modifications, was used for both the solder paste and the flux assemblies.

A forced nitrogen convection oven was used for reflow and soldering of the assembled components as shown in Figure 3.

![Figure 3: Reflow Profile Used](image)
OBSERVATIONS AND ANALYSIS

Inspection of the paste deposits indicated good print quality in terms of paste registration and print definition. The solder deposits were photographed for documentation. The assembled packages were monitored using an edge finger connector region on the board. Probe testing of the assemblies showed that all the solder joints were electrically good. X-ray evaluation did not show any solder bridging or solder balling defects. However, the assemblies showed presence of voids in the via-in-pad solder joints. The voids were found to be present for both the cases of solder paste and flux assemblies and were distributed on and around via openings. Some of the voids in the via-in-pad solder joints were located right above the via opening and were difficult to detect during x-ray evaluation.

Cross sectioning of representative assemblies was done to study solder joint quality, component standoff, wetting of pads, and the presence of any defects like voids, micro cracks, and insufficient wetting. Figures 4a and 4b are cross-sections of packages assembled on conventional and the via-in-pad structures using solder paste. The solder joints on the conventional pads showed excellent wetting and solder joint shape. For the via-in-pad joints, voids were seen at the entrance of the vias in most of the solder joints. These voids were as big as the via diameter. Note that even for the components assembled using flux, the solder joints showed the presence of voids above the via. Some solder joints however, showed the presence of voids towards the component side (Figure 4b).

![Figure 4: Solder Joint Cross-Sections](image)

There was a noticeable trend in increase in standoff as the pad diameter decreased for flux assemblies. As the pad diameter decreases, the amount of solderable pad area decreases, thus, the amount of collapse of the solder bump is different for these pad diameters. For the solder paste assemblies, as the pad diameter decreases, the amount of solder paste deposited also decreases; thus, there is no significant decrease in standoff (Figure 5). Standoff values were measured using a laser profilometer and by cross sectional analysis.

![Figure 5: Measured Stand-Off](image)

RELIABILITY ANALYSIS

Reliability of an electronic assembly or an individual component is "the ability to function for an expected period of time without exceeding an expected acceptable failure probability". Accelerated testing is one of the more common methods that are used to test the reliability of electronic components. The goal is to accelerate the time-dependent wear out failure mechanism and the accumulation of damage that reduces the time to failure. The samples that were assembled were subject to air-to-air thermal cycling using a 20 minute 0°C to 100°C cycle with a 5 minute dwell and a 5 minute ramp. Continuous electrical monitoring of the assemblies was done during cycling to find out the exact failure cycle. Data acquisition and storage were done by using an event detector and Datalog software. The resistance threshold was preset at 300 Ω. If the coupon overshot this value, an event was reported. (An assembly was said to have failed at a particular cycle ‘n’, if it is open for 10 cycles between cycle number ‘n’ and cycle number 1.1n, beginning at cycle ‘n’). Once a package was found to have failed, it was electrically probed to locate the failed joints and then an electrical mapping of the failure joint location was done. Cross sectioning was carried out, and the sections were examined using a metallographic microscope.

Data analysis was done using lognormal and Weibull testing (2-parameter, 3-parameter, Bi-Weibull). The cycles to failure
data was fitted to a 2P Weibull distribution using WinSmith Weibull software. The failure data underwent the following hypothesis:

- The reliability of the assemblies on the conventional pad was as good as the reliability on the via-in-pad structures;
- The reliability of samples assembled using flux was as good as the reliability of assemblies using solder paste.

Finally, conclusions were drawn based on the hypothesis testing results.

**Results and Failure Analysis**

- Of the 72 packages sent for testing, one sample showed very early failure at 309 cycles. This package was assembled on a 13 mil conventional pad using solder paste. Cross sectional analysis did not show any noticeable cause for early failure. The remaining packages show a characteristic life of 3143 cycles (Figure 6).

- The packages assembled on the via-in-pad structures showed Eta (N63) value of 3123 cycles while those assembled on conventional pad had an Eta value of 2798 cycles. Figure 7 shows the Weibull plot of the packages tested. Hypothesis analysis showed that the reliability of the via-in-pad assemblies was significantly more than the reliability of packages on the conventional pad. Sample t-test statistics are mentioned in Table 2.

**Figures 6 & 7: Weibull Plot – All CSPs, Via in pad**

- With decreasing pad diameter, the solder joint reliability was seen to increase (Figure 8). Smaller pads increase standoff and trace routing density [Primavera, 1999]. The pad diameter could be decreased with a corresponding result of increase in standoff and reliability up to a certain limit beyond which placement yield is affected. It was shown that by decreasing the pad diameter from 15 mils to 11 mils the Eta was increased in value by more than 40%. Hypothesis analysis showed that the reliability of packages assembled on the 11 mil pad was significantly more than the reliability of packages on the 15 mil pads. The t-test statistics are mentioned in Table 2.

**Figure 8: Weibull Plot - Pad Diameters**

- There was no significant difference in reliability between packages assembled using solder paste and flux, although the flux assemblies showed slightly higher number of cycles to failure. Cross-sectional analysis revealed that the package failure mode was of a solder fatigue type. This fatigue failure happened in the solder near the component side, independent of the board pad size or type (Figure 9). Immature of the pad type, the cracks were very fine and originated from the solder joint corners and moved towards the solder joint center, indicating fatigue type cracks.

**Figure 9: Cross Section of Failed Solder Joints**
Electrical mapping of the failed samples showed that most of the solder joints showing failures were located at the corner of the package. This is due to the fact that the distance to neutral point (DNP) was the maximum for these solder joints. The CTE of the package, in this case the silicon with polyimide, was in the 4-5 ppm/°C, while the CTE of the board was in the 14-16 ppm/°C range.

Dye penetration tests were carried out supported the observations made by cross sectional analysis and electrical mapping as shown in Figure 10.

**CONCLUSIONS**

This research effort generated a substantial quality of knowledge regarding the effects of use of solder paste and flux, pad diameter and the use of via-in-pad structures on the CSP assembly process as well as the reliability of the package. The results of this experiment can be summarized as follows.

- A total of 96 wafer level packages (4416 solder joints, of which 2208 via-in-pad) were successfully assembled.
- The reliability of the test package was found to be exceed 1000 cycles 0 to 100°C.
- The solder joints assembled on the via-in-pad pads were equivalent to conventional pads;
- Increased standoff resulted in higher reliability. By decreasing the pad diameter from 15 mils to 11 mils the characteristic life increased 40%
- The via-in-pad solder joints showed the presence of a void at the via opening. However, the presence of this void did not affect the reliability of the solder joint;

Although the above observations are specific to the package assembled and evaluated, some of the conclusions can be generically applied to CSP assembly and reliability.

**REFERENCES**


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Table 1

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Table 2