

# INFLUENCE OF PCB PARAMETERS ON CHIP SCALE PACKAGE ASSEMBLY AND RELIABILITY

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## ABSTRACT

*While the electronics industry continues to strive towards miniaturization, it is important to understand the fundamental issues that are a result of the increased package density. Current standard surface mount devices such as peripheral leaded packages and area array (Ball Grid Array) devices offer robust assembly yields and good long term solder joint reliability. When developing a new device or packaging method, it is critical that these must compare to or perform better than standard devices. Not only should the new device perform well in assembly, they must show acceptable package and solder joint reliability in order to gain acceptance and wide use. In an attempt to achieve the functionality and density of bare die assembly, a series of devices known as Chip Scale Packages (CSP), have been developed by the packaging industry which are very close to the dimensions of the bare silicon die. While CSPs have been used extensively in low I/O areas such as memory applications, use of CSPs in more demanding environments and applications has been adopted less readily. This paper describes some of the fundamental issues associated with CSP package reliability. Specifically, assembly process parameters, material selection and board geometry affect the yields and reliability during attachment of CSPs onto organic motherboards. Factors such as presence of voids, reflow atmosphere, attachment pad metallurgy and assembly parameters such as solder paste or flux, show dramatic differences in accelerated thermal cycle testing. This paper discusses some of the basic assembly and Printed Circuit Board (PCB) parameters that influence the success of CSP assembly and solder joint robustness. CSPs have been assembled using conventional surface mount techniques and the long-term solder joint reliability has been assessed using accelerated thermal cycle testing and various mechanical testing methods. Reliability modeling has been performed using the finite element method to compare predicted fatigue lives with test data from both 0-100C and -40-125C thermal cycles. CSPs have emerged as an area array packaging alternative for applications requiring low to medium input / output counts on limited Printed Circuit Board (PCB) real estate. Due to their leadless (in general) configuration, larger ball pitch, and compatibility with existing standard surface mount PCB assembly equipment, CSPs avoid a significant segment of the assembly problems encountered in fine pitch peripheral leaded device assembly. However, while the use of CSPs has been steadily increasing, it is not considered significantly widespread beyond memory device applications. The explosive growth in CSP development in recent months has been fueled by the promise of high assembly yields and low package cost. The trend towards minimal package design is apparent with the release of numerous wafer scale packages, which are often Si die with one or more redistribution layers. One significant issue concerning CSP as well as ball grid array (BGA) process development has been in the area of joint quality and inspection. Often area array devices are suspect in the test and burn in stage of production due to the inability to visually inspect the joints. While transmission X-ray inspection can assist in inspection of joint related parameters such as voids, the impact on joint integrity is difficult to measure. This paper addresses some of the PCB factors that influence the reliability of area array devices, in particular CSPs.*

**Keywords:** Printed Circuit Boards, Area Array Components, Chip Scale Packages, Ball Grid Arrays, and Reliability

## INTRODUCTION

With the continual miniaturization of electronic components and overall systems, the interconnection between the printed circuit board (PCB) and the component, namely the solder joint becomes smaller as well. This reduction in the physical size of the joint places more demands on the mechanical properties of the solder to ensure joint robustness. In addition to the footprint size reduction, there is an emphasis on total space reduction, often in the form of reduced size in the packaging of the silicon die. As surface mount technology (SMT) migrates towards smaller package dimensions, the physical and thermal characteristics of each

material used in the packaging becomes more critical. Very large differences between properties within a package for example layer to layer, as well as between the carrier and the die lead to large internal stresses within a package. Once mounted onto a PCB, the solder joint must typically absorb all strains induced by the expansion of the package and PCB in thermal excursions. For traditional SMT devices, such as quad flat packages, the leads as well as the solder joints provide the compliance needed to compensate for the mismatch in coefficient in thermal expansion (CTE) of the package and PCB. However, in area array devices such as ball grid array (BGA) and chip scale packages (CSP), the joint alone must provide CTE mismatch compliance. The smaller the joint becomes, the more critical the joint quality

becomes. Physical defects such as poor solderability, excessive intermetallic formation, and voids can negatively impact joint robustness and soldering yields. Voids are cavities and bubbles that form within the solidified solder, and may weaken the joint in mechanical, thermal and electrical properties [1].

## 1.0 ASSEMBLY FACTORS CATEGORIES

Factors that affect the assembly and reliability of CSPs are similar to the parameters that affect BGA assembly and reliability. Since most CSPs are smaller versions of BGA packages, the critical parameters that affect BGA should be the same as for CSPs. As shown in [2], factors that affect area array assembly yields can be classified into several main categories including;

Assembly Materials  
PCBs and Components  
Process Methods  
Resulting Joint Quality  
Human Factors.

The “Assembly Materials” category can be further subdivided into solder paste and flux related parameters such as applied volume, reflow parameters, fluxing and solder paste deposition methods, and handling & storage conditions. The most critical issue of this category is to ensure proper fluxing of the attachment surfaces and creation of proper metallurgical bonds during the reflow operation.

The “PCB” category contains many influential factors on the overall solder joint reliability including: pad metallurgy, board thickness, pad size, base material, via formation technology, routing method (via in pad versus fan out), PCB layer count, soldermask technology, and pad definition versus mask definition. The PCB parameters that influence CSP reliability will be the focus of this paper. The “components” sub-group parameters that influences the assembly reliability may include; construction (flex versus rigid carrier etc.), die size to package ratio, solderball size, attachment pad size and definition, base materials, package size, and ball configuration.

The “Process Methods” category is heavily influenced by the individual steps in the assembly; for example, standard double side assembly or a mixed assembly with solder wave pass. Influence of factors such as reflow methodology, (convection, versus InfraRed (IR) radiation), and atmosphere will affect solder wetting, joint formation / shape, and the presence of voids. Resulting joint quality is a function of almost all assembly variables but is strongly influenced by the type of paste/flux, attachment pad metallurgy and reflow conditions. Highly irregular shaped joints; excessive voiding and poor solderability may lead to early failures. Human factors that are often overlooked may include operator education and training in addition to human error.

## 2.0 CRITICAL PARAMETERS

One advantage of the CSP package is its compatibility with the existing standard surface mount PCB assembly environment. Typically, current CSP assembly process rely on solder paste deposition through stencil printing, component placement, and mass reflow soldering. In order to ensure high process yields for the assembly process, process parameters that relate to all the above mentioned operations need to be considered. Factors that could affect the assembly process yield can be divided into four main categories including Human Factors, Equipment and tooling, Materials, and Process Methods. These four categories and their sub-categories are briefly described in the following sections. Figure 1 illustrates the cause and effect diagram (fish bone diagram) that can be used to illustrate the factors that influence CSP assembly yields.

### 2.1 Human Factors

Input from operators (including human error) is one of the contributors that can affect the yield of the assembly process. Factors that impact this category include handling, training, education, setup and quality control.

#### 2.1.1 Handling

Improper handling (manual and/or automated) can be detrimental to the integrity of components on the assembly. This issue becomes extremely important when automatic assembly transportation systems (conveyor) are not implemented. Improper manual handling (especially after the component placement process) may result in component misalignment. Consequently, defects such as opens or bridges can occur after reflow soldering. When handling moisture sensitive packages, adequate handling strategies should be implemented to prevent devices from excessive moisture absorption or damage to circuitry. Popcorning of the device can commonly be attributed to the rapid expansion of entrapped moisture during exposure to high temperatures. Ideally, the device should survive several reflow cycles after being exposed to factory floor conditions during normal scheduled assembly production. Diffusion of moisture into area arrays typically follows Ficks law of diffusion, however solving the multilayer diffusion problem (diffusion through more than 1 surface layer, as well as the exposed ends of the substrate) requires all material properties to be known. Therefore, it is usually necessary to determine the moisture sensitivity for each type of package. Moisture desorption, or bake out requirements, need to be measured for each device type as well. Moisture sensitive components may require a pre assembly bake out in addition to storage in a dry nitrogen chamber. In general, CSPs show almost complete moisture desorption following a 4 hour bake out at 125C. However, larger devices and moisture sensitive BGAs require bake out at typically 125C for as much as 24 hours. Figure 2 shows a typical CSP desorption cycle for a 125C bake.

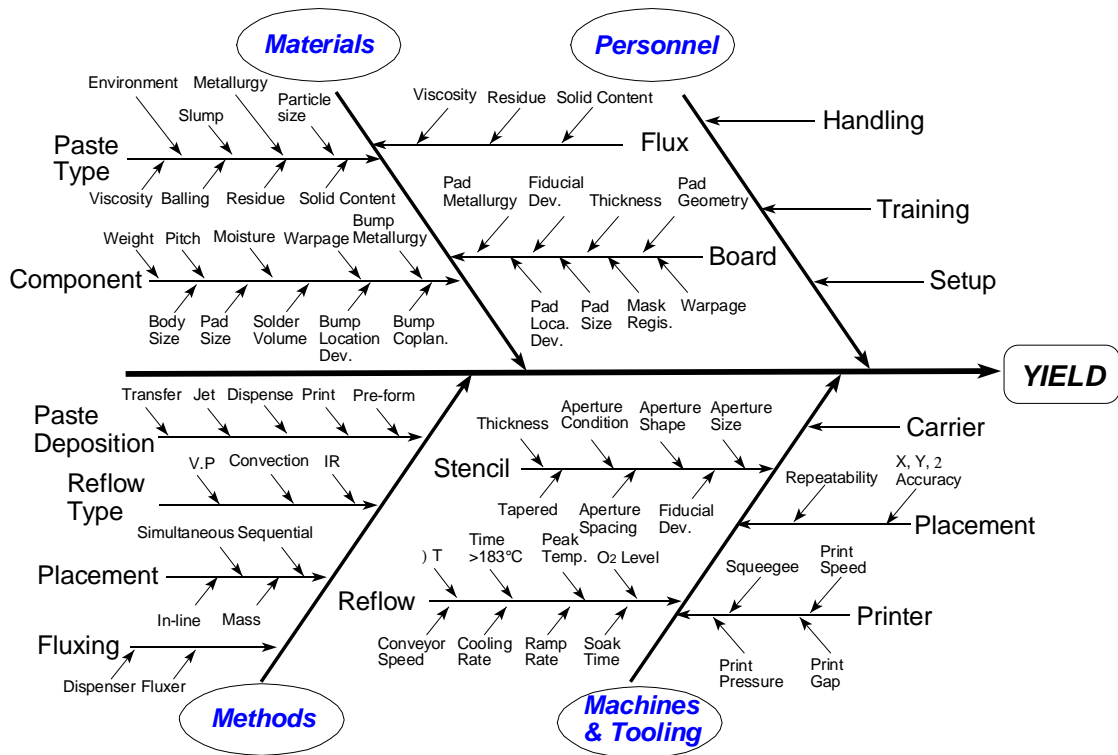


Figure 1: Assembly Yield Cause and Effect Diagram

### 2.1.2 Setup & Quality Control

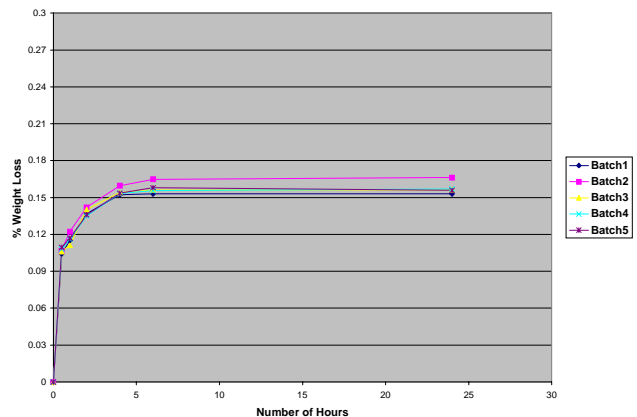
Correct setup of the equipment is very important to ensure high throughput and yield. A machine's setup does impact the consistency and accuracy of the results obtained. The setup used at every stage of the PCB assembly process needs to be thoroughly reviewed by domain experts and properly validated. Gage studies should be performed to maintain consistency from line to line and operator to operator. Simple procedures can be implemented to assess the performance of the equipment and operators, these include stencil printing onto a bare laminate before each shift, placing test components onto double sided taped boards, and using a data logger with a thermocoupled board in the reflow oven on a regular basis. More advanced methods could implement assembly of test boards, in process measurement of process variables, and characterization of the placement machine with precision chrome / glass components and boards.

### 2.1.3 Training & Education

Operator training not only should focus on equipment, but needs to be extended to include assembly process, and general surface mount issues. Familiarity with the overall process can often help the operators associate with what happens down line from their operation. Mistakes and improper education can affect subsequent operations, and the operators must be able to understand the result. Human error can be minimized by a combination of training, proper equipment and tools, and attitude. Often operators assume the end product can be reworked if they do not assemble the product properly the first time, this could be a costly attitude

to take.

FIGURE 2 - CSP Description Curve



## 2.2 Methods

The typical assembly process for surface mount area array devices could consist of solder or flux deposition, component placement, reflow soldering, and transportation. The methods used for each individual operation are described below.

### 2.2.1 Solder Deposition

In CSP assembly, both paste deposition and pre-formed solder spheres are used to create a solder interconnection between the package and the PCB. Most CSPs utilize a eutectic or near eutectic Sn/Pb solder alloy. Some CSPs and

BGA components may utilize a high melting (above 300C) solder alloy (5/95 Sn/Pb) solder balls to prevent the device from collapsing during solder reflow. The eutectic BGA device spheres melt during a standard reflow process and collapse to an equilibrium state. Equilibrium is achieved with the balance between package weight and the buoyant force of molten solder surface tension. With eutectic CSPs, there is a sufficient amount of solder in the component ball to provide interconnection, however, coplanarity of the device becomes critical to ensure that each bump forms a proper joint.

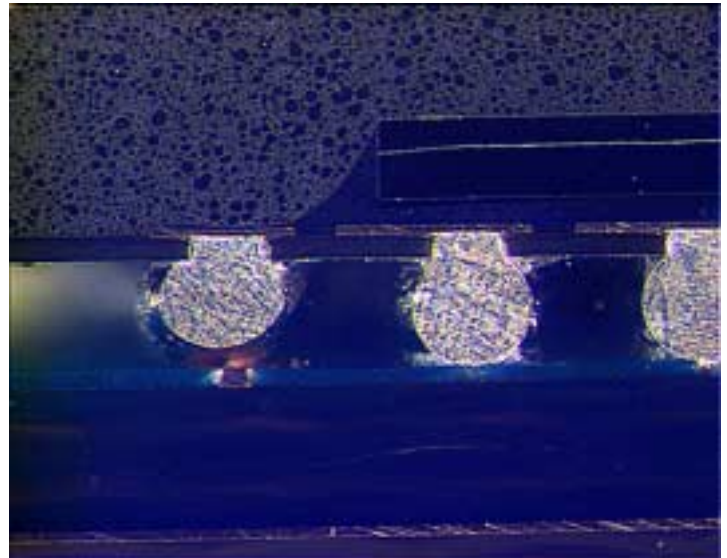
The most common method for solder deposition in CSP/BGA assembly is solder paste stencil printing. In this process, solder paste is deposited onto the attachment pads of the board through corresponding holes made in a metal foil. For fine pitch CSPs, the printing process becomes critical since there is insufficient room to elongate the solder stencil apertures. Printing circular features greatly reduces the amount of paste transferred through the aperture. For 0.5 mm pitch CSPs, it is not uncommon to achieve a print efficiency of less than 60%. Aperture size and stencil thickness needs to be properly adjusted to ensure the highest transfer ratio (paste deposited versus aperture volume). In general, the apertures should be slightly oversized compared to the attachment pad geometry to increase the solder deposit volume and transfer ratio. However, this may lead to an increase in solderball and satellite formation. Nitrogen may help counteract the tendency of the paste to form solderball during paste overprinting.

### 2.2.2 Fluxing

Since it is possible to attach collapsible (eutectic) CSP/BGAs without solder paste, attachment methods may additionally include flux deposition. Fluxing for CSPs can be achieved by dipping the component into a flux film deposit, dispensing, spraying, and brush methods. In order to minimize the flux residue left on the PCB following reflow, methods that deposit flux only in the needed areas should be considered. Dipping is commonly used to flux the component balls. In this method, the device ball planarity must be considered when specifying the dip depth. The dip depth must be at least 1 mil (0.0254mm) larger than the ball coplanarity to ensure each bump is fluxed. The flux cleans oxides from the surfaces during the reflow operation.

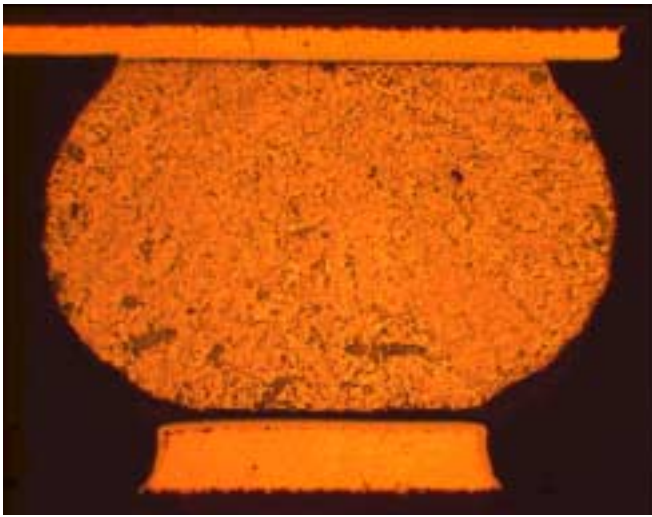
Fluxless methods rely on oxide removal prior to assembly, typically in a plasma cleaning system. In plasma systems, an impinging plasma gas bonds with the oxygen molecules on the surface of the sample, and are removed leaving a clean exposed surface. However, the solder paste and or flux are used to retain the component in place during the assembly and transportation of the PCBs. The tackiness of the flux / paste required will depend on the assembly process used. In-line automated assembly will require less retention force than manual batch assembly. Additionally, placement equipment utilizing table movement rather than head movement will require much larger retention forces due to high accelerations imposed on the PCB and component.

When a flux only method is used for CSP assembly or rework operations, it is critical to ensure that both the bump coplanarity and warpage of the assembly at reflow temperature is fully understood. The combination of variation in solder ball volume and warpage of both the package and substrate may lead to solder joint opens. If a package has a "small" ball and the device has significant warpage during the reflow, there may not be sufficient solder volume to form a proper joint during the bump collapse. Figure 3, shows an assembly with an open joint due to a combination of package warpage and insufficient solder ball volume.



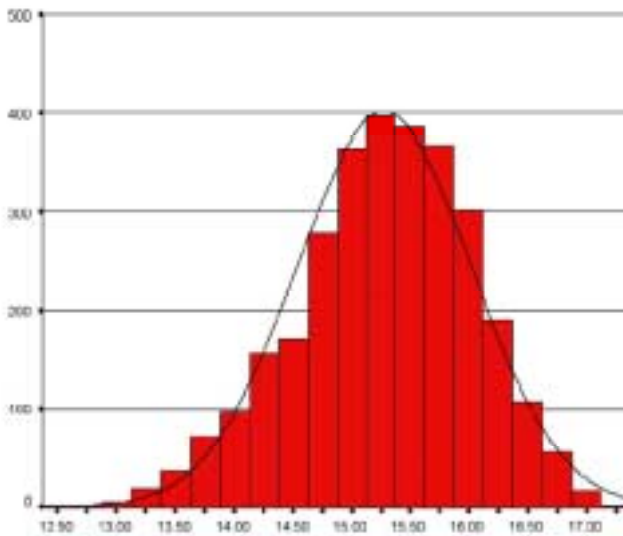
**Figure 3 - Small Ball CSP Open**

The device is a commercially available 144 I/O flexible carrier wirebond CSP with a 0.8 mm pitch. In many cases, the addition of solder paste will help minimize the "small ball" open since the reflowed paste can help bridge the gap between the component bump and the PCB attachment pad. In addition, a flux only process can result in a marginal or cold solder joint if the flux is applied in too low a volume. In the case of high bump coplanarity, the flux may not sufficiently coat the shortest bump tip and be unable to remove all the oxides during reflow. If incomplete fluxing occurs, a complete metallurgical bond may not form. Marginal / weak joints results in early failure during thermal cycle testing. Figure 4, shows a device failure at the component ball to PCB pad interface due to poor wetting. This device was assembled using a 2.5 mil (0.0635mm) thick flux film. To understand the effect of bump coplanarity on assembly / joint formation, experiments were performed to determine the level of bump coplanarity and package warpage that would lead to open solder joints. During the experimentation, flux depth was varied from 2.0 to and 4.5 mils (0.05 - 0.114mm) in thickness.



**Figure 4 - Non-wetting / small ball open**

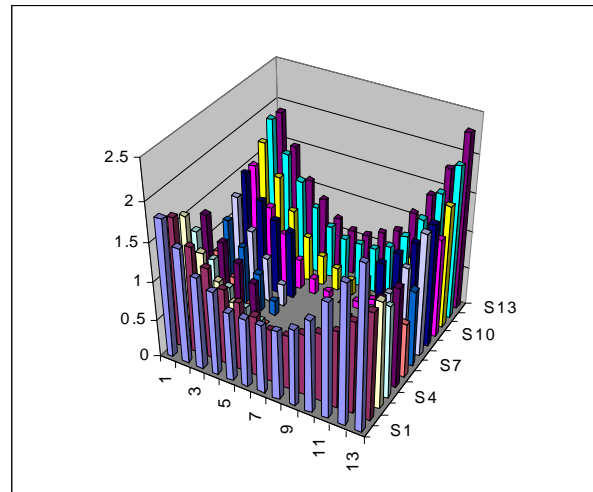
The device coplanarity was measured for samples as shown in the bump height distribution of Figure 5. The package warpage was measured by several techniques including; moiré, laser profilometry, and interferometers found in [3].



**Figure 5 - Ball Height Distribution**

Shown in Figure 5 is a histogram of measured ball height for a 0.8 mm pitch CSP. Sample size is 3024 with the mean height 15.2 mils (0.386mm) and one standard deviation of 0.75 mils (0.02mm). A representative warpage plot for the device is shown in Figure 6. The experiment showed that for the device studied, a flux film of less than 3.5 mils (0.09mm) resulted in either cold joints, or opens. This is not surprising since the bump height distribution for the device and the warpage of the device are large. By repeating this experiment for many device types, it was found that in general, the ball coplanarity for a CSP should be less than the following: 3.0 mils (0.076mm) total ball diameter variation at 3 sigma (0.5 mil (0.0127mm) for 1 standard

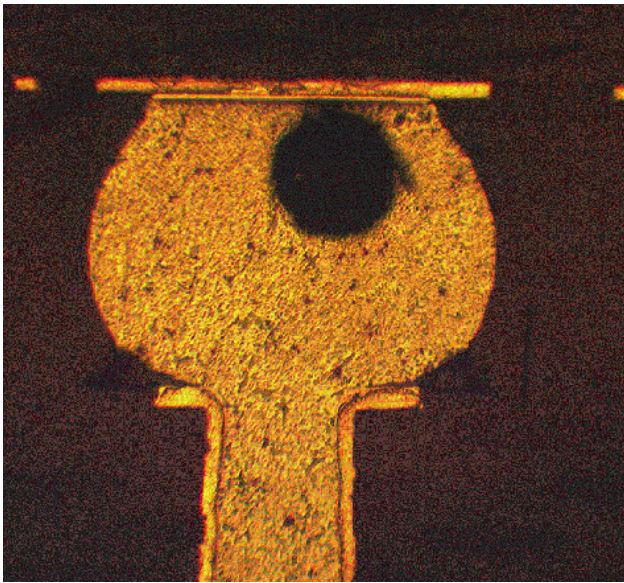
deviation) combined with a reflow temperature package warpage of 2 mils (0.05mm). Warpage measurement techniques are further detailed in [3].



**Figure 6 - CSP Device Substrate Warpage Measurement**

### 2.2.3 Reflow Soldering

The heat transfer mechanisms used in the mass reflow soldering process include convection, radiation (using infrared sources), and condensation (vapor phase). The most popular method of reflowing solder is based on forced convection and/or IR radiation. Some other methods of solder reflow are vapor phase, laser, and hot bar. In addition to mass reflow soldering, PCBs are often subjected to a wave soldering operation. In wave solder applications, the PCB is passed over a molten wave of solder. As the board passes over the wave, solder is attracted to all wettable surfaces including attachment pads, component leads, and vias. When CSP/BGAs are populated onto boards with mixed technology, special process concerns arise. High I/O area arrays may require a significant number of vias on the PCB. Since both heat and solder can be wicked into the via, special precautions must be imposed when subjecting a PCB populated with BGAs to a back side wave pass as shown in [4]. Wave temperature must be carefully controlled to prevent the top side solder joints from secondary reflow. The higher the via density, the more heat transfer occurs, and thus more temperature control performed. Taping the bottom side via area with a polyimide film, or use of peelable temporary masks will minimize top side reflow and solder to be wicked into the via. Additionally, the top side via pad should ideally be covered with solder mask to prevent the solder ball from misplacement or wicking into the via shown in Figure 7.



**Figure 7 - Assembly Reflow on Through Hole**

Uniformity of temperature across the PCB and within a component is a primary goal of any reflow system. For area array devices, a temperature gradient of 10C or less should be maintained to prevent warpage of the package and to ensure all joints reflow properly. For small CSPs it was found that infrared reflow systems are sufficient to maintain less than a 10C gradient. However IR reflow of BGAs have much larger temperature gradients across the PCB and package due to color differences, surface emissivity of the devices, and shadow effects. Cold joints can form if a very large temperature gradient occurs. Warpage is a major concern for BGA reflow as well. Preferential heating, shadow effects, and highly reflective surfaces can cause package warpage, bridges, and opens to occur in BGAs. By contrast, forced convection reflow provides a substantially lower temperature gradient across the PCB and BGA solder joint array than infrared furnaces. For additional issues related to the reflow of BGAs and how it affects assembly yields, see [5], [6] or [2].

#### 2.2.4 Placement

The strategies used to place components on boards can be divided into in-line, mass, sequential, and simultaneous placement. In very high volume manufacturing, dedicated sequential or mass placement may be performed. In most cases, flexibility is important to accommodate new products and components. Typically, CSP assembly utilizes sequential component placement. Two types of placement equipment are used for sequential pick and place operations, the first is an X,Y gantry style, and the second is fixed head moving table placement machines. The overhead equipment offers high flexibility, medium placement speed, high accuracy, and minimal accelerations or movement of the PCB. In contrast, the table movement machines (usually rotary turret heads) offer very high placement speeds,

medium accuracy, medium flexibility, and impose high accelerations on the PCB.

Another important feature of the placement equipment that affects CSP assembly is the equipment vision system. A major issue is the ability of the equipment to recognize features on the board and component and accurately place the device by aligning the device bumps to the attachment pads on the PCB. Another important aspect of the vision system relates to the mis-identification of device features. Some CSPs have logos, nomenclature or other features on the array side of the device. These features may be misinterpreted as a ball location by a standard forward illuminating camera. Illumination of the package from a lower angle, namely side lighting, may be required to prevent erroneous ball finds on CSPs with bottom side non-ball features.

### 2.3 Materials

The materials used in the surface mount area array assembly process include solder paste, stencils, components, flux, and the PCB.

#### 2.3.1 Solder Paste

The wet solder paste, after being deposited on the pads on the board, holds the components in place prior to the formation of the solder joint (by reflow soldering). The solder paste, at this stage, temporarily acts as an adhesive. Characteristics of the solder paste that are important from a process perspective include; the solder powder particle size, metallurgy, slump, temperature and humidity sensitivity, solids content, type of flux residue, viscosity, and the propensity for solder balling. No-clean eutectic (63/37 Sn/Pb) solder pastes with high metal content (approximately 90 percent by weight) are widely used in CSP/BGA assembly. The solder paste used for SMT assembly needs to be subjected to a battery of tests. These tests, as outlined in [7], and the results obtained help to ensure the quality of the solder pastes used. The tests that need to be conducted include some specified by the IPC (as discussed in IPC-SF-818 and IPC-SP-819) while the rest are standard tests adopted by the electronics assembly industry. The tests that are used to evaluate candidate solder pastes include the solder paste viscosity test, the solder balling test, the solder paste slump test, the wettability, the tack strength, the printability, the spread test, the copper mirror test, the surface insulation resistance test, and the electrochemical migration test.

While the basic characteristics of the solder paste can be confirmed through exhaustive testing, the choice of the particle size used in the solder powder for area array is dependent on device pitch. For the assembly of standard BGAs (1.27 mm), the stencil aperture size is typically 0.55 to 0.65 mm in diameter. A solder powders particle size could range from Type 2 (-200/+325 mesh size) to Type 4 (-400/+500 mesh size). As the device pitch decreases, the aperture size will correspondingly shrink. For 0.8 to 1.0 mm pitch the device aperture size is typically 0.4 to 0.5 mm and

thus requires a Type III paste. As the pitch is further reduced, a Type IV paste should be used. In assembly of 0.5 mm pitch, the aperture size may be as small as 0.25 to 0.35 mm. The ability of the solder paste to successfully transfer through the stencil apertures will be influenced by several paste properties including particle size distribution. A series of experiments were performed to determine the effect of paste Type on transfer efficiency. Two pastes were compared (Type III versus IV). Printing was accomplished using an automated stencil printer and solder paste deposition was measured using a SVS7530 paste inspection system. Two stencil thicknesses were compared 5 mils (0.127 mm) versus 6 mils (0.15 mm). The aperture size was varied between 10 mils (0.25 mm) and 13 mils (0.33 mm). Printing was performed on 20 panels with 4 devices each, by printing a single board, performing inspection, cleaning the board and reprinting. The results are summarized in Table 1. On average, the Type IV paste gave 10-15% higher paste transfer efficiencies than the Type III. In addition, a dramatic effect was observed for the stencil thickness. Table 1 shows the "best" resulting combination of parameters for this experiment, Type IV, 0.17 mil apertures and 5 mil thick stencils. Similar experiments were performed using 12 commercially available no-clean solder pastes, to study the effects of aperture shape and size.

Paste	Device	Transfer Ratio	
		Thickness (aperture) mils	Nominal volume = 1/4BHD <sup>2</sup>
	0.5mm pitch 46I/O		
1 - No clean Type IV	1	44% - 6 (11)	70% - 5 (13)
	2	54% - 6 (11)	64% - 5 (13)
	3	34% - 6 (10)	40% - 5 (10)
	4	37% - 6 (10)	49% - 5 (10)
2 - No clean Type III	1	40% - 6 (11)	66% - 5 (13)
	2	49% - 6 (11)	61% - 5 (13)
	3	27% - 6 (10)	30% - 5 (10)
	4	37% - 6 (10)	44% - 5 (10)

**Table 1 - Printing Transfer Efficiency**

### 2.3.2 Fluxes

Since the application of flux may be appropriate for CSP assembly or rework, important flux characteristics including viscosity, flux residue, and solids content should be investigated. Screening tests need to be performed to identify potential flux candidates and only those that meet process requirements should be selected.

### 2.3.3 Components

CSP components are available in different package configurations including overmolded, flex carrier, rigid carrier, and various wafer scale formats. The component related dimensional parameters include component lead pitch, warpage, bump coplanarity, bump location deviation (radial deviation), solder bump volume, pad size, and body size. Variations in these parameters would change the characteristics of the solder joint and could result in solder joint opens or satellite solder balls (with the potential for

bridging). A rigorous component handling strategy needs to be adopted. Moisture sensitive packages should be baked prior to actual use in assembly. The solder bump metallurgy of the BGAs are typically either collapsible with eutectic (or near eutectic) composition or non-collapsible with high lead (Sn/Pb 10/90) composition. This characteristic changes the level of significance of each dimensional aspect. When eutectic solder bumps reach the liquidous temperature of the alloy during reflow, they collapse. At the equilibrium state, each solder joint acts like a spring and the sum of all the forces applied on all the solder joints is zero. The solder joint standoff is, typically, less than the original solder bump height. Therefore, the variation of the solder bump height is somewhat compromised.

CSPs serve the fundamental purposes of any IC package. They provide a metallurgical interconnection between aluminum die bond pads and the solderable metallurgy of a PCB. Simultaneously, CSPs deliver a geometric rearrangement of the IC's bond pads, often resulting in a more relaxed I/O pitch compared to the die bond pads. A CSP is defined as the following:

1. A package that occupies no more than 1.5 times the area (footprint) of the die
2. The individual side geometry is no more than 1.2 times that of the corresponding chip side dimension
3. Package that is direct surface mountable as opposed to the use of wire bonding.

Typically, CSPs provide electrical connections to the PCB in array patterns, on pitches less than 1.0 mm. While the CSP seems to offer abundant advantages, long term component and solder joint reliability must be fully understood. The lack of published data and limited use of CSPs to date prompt the question of package integrity. By design, the package is only slightly larger than the silicon die, thus creating a large thermal expansion mismatch between the device and the PCB laminate. From a reliability standpoint, there are only two types of CSPs, mechanically and non-mechanically decoupled devices. Many of the devices utilize an interconnecting ball pattern that is referred to as a Chip Scale Grid Array (CSGA) [8]. However, from a generic classification of CSPs, they are typically classified into the following five categories:

- A. Interposers with a flex circuit interconnect.
- B. Interposers with rigid substrates.
- C. Lead on Chip (LOC).
- D. Wafer-level assembly packages.
- E. Wafer-level processes with redistribution.

#### 2.3.3.1 Flexible Carrier Devices (Elastomer Interposer)

This style package incorporates a flexible circuit rerouting technique to connect the die bond pads to the solder bumps of the CSGA [8]. The overlay is adhered to the die face with the back of the die exposed. The sides of the die can be exposed or covered with a protective material for handling purposes. Examples of this CSP type are the Tessera

“Micro-BGA” [9], the Chip on Flex package by General Electric, FlexCSP by Amkor, MicroStar by Texas Instruments, as well as a center pad memory module CSP by Texas Instruments [10].

### 2.3.3.2 Flexible Carrier Devices (No Interposer)

A subset of the flexible interposer type CSPs, die mounted to a polymer substrate without an interposer is becoming a common package. Various types of methods are used in the construction of these types of CSPs but most utilize a polyimide flexible, metallized substrate onto which the die is attached using standard die bond epoxy. Most are wirebond but literature refers to flip chip types as well. Packages of this type include; General Electric’s Chip-on Flex, Texas Instruments wirebonded Microstar and Memory flex, PacTech’s fibre push on flex and Amkor’s Flex BGA to name a few.

### 2.3.3.3 Rigid Carrier Devices

Many CSPs are utilizing rigid substrates as interposers in an attempt to push ball grid array component technology into fine pitch / small foot print applications. These devices are typically wirebond dies mounted to a rigid ceramic or organic BGA type interposer [8]. Several flip chip die versions are being developed as well [11]. Several manufacturers are pursuing development of these devices including Matsushita’s “Land Grid Array” (LGA), Motorola’s “SLICC” (or slightly larger integrated circuit carrier), Amkor Anam’s “Chip Array” are examples of this type of CSP.

### 2.3.3.4 Lead Frame / Molded Devices

Lead on chip (LOC) technology uses mold resin and support lead frames as package constructing materials which makes the CSP retain the advantages of conventional packages while reducing the size. The technology was developed to decrease the ratios of package to die area and to facilitate the mounting of large memory devices. The other advantage is that it can use dies that are center wire bonded [12] , [10]. Hitachi Cables "Micro Stud BGA", Amkors - ChipSOP and Texas Instruments - Lead On Chip CSP packages are examples of LOC devices.

### 2.3.3.5 Wafer level Assembly Process

Various types of CSPs are manufactured in a wafer format. An example of this type of CSP is Chip Scale’s Micro-SMT package and Shell Case’s - Shell CSP, where the packaging process starts with a finished wafer. In these devices, the majority if not all of the packaging is done on the wafer level and finished devices are diced and shipped.

### 2.3.3.6 Wafer Level Redistribution Process

CSPs that are manufactured using a wafer level assembly process with redistribution layers have solder bumps that are internally connected to the die surface either by columns or by a polyimide circuit redistribution routing layer [8]. Many are a smaller version of the larger molded package types or are flip chip die with multiple polyimide layers. If the device is subsequently molded, moisture handling and

moisture absorption become a critical issue before reflow. Examples of this type of package includes Flip Chip Technologies "Ultra CSP", and National Semiconductors "Micro SMD".

Many component related parameters affect both assembly yields and reliability. Foremost is component construction. The overall material layering and resulting coefficient of thermal expansion (CTE) drastically change the solder joint reliability. In general, solder joint reliability scales with CTE. As the packaging of the die decreases, the device CTE becomes approximately that of silicon (namely 2.5 PPM/C). Wafer level CSPs have composite CTE values ranging from 3ppm/C to 5ppm/C, while laminate based CSPs have a ball side CTE of approximately 10ppm/C to 15 PPM/C. An example of the dramatic difference in resulting reliability is shown in Table 2. An experiment was performed to study the component construction versus reliability utilizing several packages constructed in the same outline, die size, and bump pattern. Results are compared for several package types. A three dimensional finite element model (FEM) was created for each package. The FEM model included creep, non-linear material properties, and temperature dependant solder. The models were created as described in [29].

Device	Sample size	0-100C N50	Beta	FEM N50 beta=4)
Flex 1	58	405	6.5	390
Flex 2	12	434	4.4	387
Flex 3	35	5300	7.9	2161
Laminate 1	6	2480	6	
Laminate 2	24	6300	8.1	4436
Lmainate 3	8	5498	7	
Ceramic	30	150	2	172

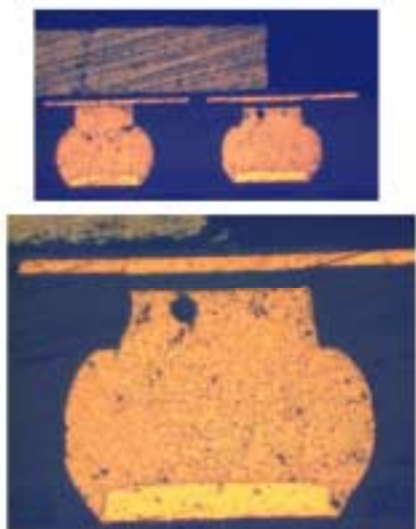
**Table 2 - 0-100C ATC results compared with FEM**

A 144 I/O 0.8 mm pitch CSP device (12 mm square with a 6.5 mm square die) was fabricated using a flex carrier, ceramic carrier and laminate carrier. Keeping as many of the remaining parameters constant, ex. Mother board, pad size, pad finish, ball size etc., the laminate packages were shown to last up to 10x longer than the flex device and 100x longer than the ceramic device during a 20 minute 0-100C ATC test. Many other parameters such as solder ball size, thickness of each layer in the package, pad definition and size, and material selection will similarly increase or decrease the subsequent device fatigue lives. Individual contributions of package parameters will be addressed in future publication(s) since it is beyond the scope of this paper.

### 2.3.4 Printed Circuit Board

Boards (substrates) made of organic materials are most commonly used in area array assembly. Board related parameters that influence the assembly yield due to variations in their dimensional parameters include: fiducial deviation, warpage, mask registration, pad size, and pad location deviation (radial deviation). To prevent pads from

oxidation, a solderable layer or coating is deposited on the pad surface. The commonly used pad coating materials include eutectic solder deposited through the Hot-Air-Solder-Leveling (HASL) process, Organic Solderability Preservative (OSP), nickel/gold, nickel / palladium, silver, and tin. These coatings, resulting in different pad finishes, may change the solderability of the pad and, consequently, affect the solder joint's quality. For properly formed joints, a metallurgical bond forms between the solder (Sn) and pad surface (Cu or Ni). During reflow, the Sn combines with Cu or Ni to form an intermetallic layer. While brittle, the layer is extremely strong. For properly formed metallurgical bonds between Cu or Ni and Sn, the interfacial strength is sufficiently higher than the plastic flow stress of the solder. In this case, the solder will rupture or fatigue during thermally induced strains. However, many problems exist that prevent the proper metallurgical reactions to occur. These may include improper amounts of co-deposition materials in the plating baths, oxidation of the underlying pad surface, porosity in the outermost cover layer, organic contamination, soldermask residue, or improper fluxing. This problem will often lead to poor adhesion of the solder ball to the attachment pad. This can result in a very low ball attachment yield, missing solder bumps, time zero joint failures (including dewetting) or weak interfacial strength. In the case of weak interfacial strength, the plastic flow stress of the solder is higher than the interfacial strength and small thermally or mechanically induced strains will cause the solder ball to detach from the pad surface as shown in Figure 8. This can be common with the Ni/Au attachment pad metallurgy. Assembly of approximately 2 million solder joints (BGA & CSP) during this research lead to more than 50 time zero failures on packages. However, packages utilized in this work were a mixture of commercially available devices, pre-production parts, and daisy chained packages. Therefore, these packages may not fully represent true production CSP devices.



**Figure 8 - Time Zero CSP Component Side Failure**

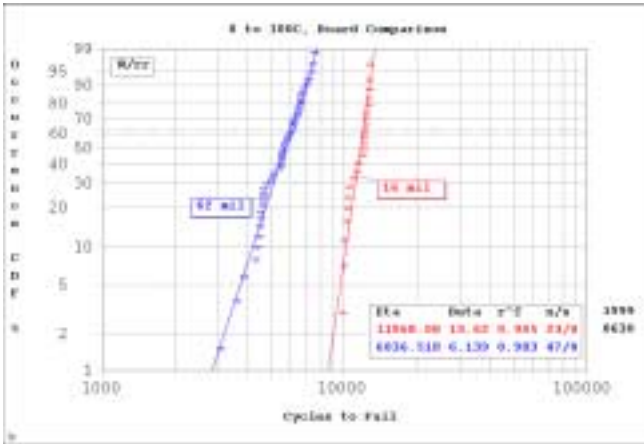
The time zero failure often associated with Ni/Au pads, can be problematic to detect since the solderball appears to be firmly attached to the pad. In fact, the ball shear strength required to remove a solder ball with a marginal solder attachment may have an equally high peak shear strength when compared to a “good” joint. A complete load-displacement shear curve can be obtained by a ball shear test in order to evaluate the ball / pad interface [13]. It is very important to realize that the “time zero” solder failure is not caused by the same mechanism as joints that embrittle with exposure to elevated temperature. In the later case, the joint degrades well after assembly and only after exposure to elevated temperatures (>100C). Many theories have emerged as to the origins of the high temperature degradation [13], [14 ], [15], [16], [17] and [18]. It is critical to determine the source of the failure, because poor pad coating can result in solderability problems.

The attachment pad geometry can be defined by its pattern (pad defined) or by the solder mask opening (solder mask defined). The thickness of the board and the materials used in each layer will change the overall stiffness of the board. This could influence its warpage or sagging during the assembly process.

Many PCB Parameters affect reliability of the CSP assembly. Of the various parameters, the board thickness, pad size, pad definition, and attachment pad metallurgy is the most influential. A drastic increase in CSP solder joint fatigue lives can be realized by use of a "thin" PCB. When comparing the reliability of CSPs assembled onto 0.062" (1.575 mm) PCBs versus assemblies on 0.016" (0.4mm) thick PCBs, there is as much as a 2x difference in fatigue lives. An example of this dramatic difference in reliability is shown in Figure 9. The data is shown for a 160 I/O 0.8 mm pitch laminate carrier CSP assembled onto tetrafunctional FR4 PCBs. The data was generated using a 0-100C ATC test with 5 minute ramp and 5 minute dwell times. Event detection, electrical mapping, dye penetration and cross sectioning methods were used to identify failures. The assembly process for the devices included: solder paste printing using a 5.0 mil (0.127mm) thick stencil, placement by an overhead gantry pick and place machine, and reflow in a nitrogen (less than 50 PPM O<sub>2</sub>) convection reflow oven.

Another equally important PCB parameter that can influence assembly and reliability is the attachment pad size. There is a direct trade-off between yields and reliability when changing pad size. Large attachment pads lead to larger ball collapse and thus can accommodate a much larger ball coplanarity and package warpage. In addition, the placement, self centering of the device, and stencil printing is more robust for large pads. However, that larger pad reduces the effective standoff height for the solder joints. The shear strain imposed on a solder joint is related to the shear angle that the joint is forced to undergo during thermal excursions. A mismatch in the device and motherboard CTE cause thermally induced strains in the solder joints.

**Figure 9 - Weibull Distribution - PCB Thickness Effect, Sample 1 - 0.062" PCB (N63 = 6036, Beta = 6.14) Sample 2 - 0.016" PCB (N63 = 11,968, Beta = 13.6)**



The farther away the package is from the board surface, the smaller the shear angle for the same thermal displacement. IBM's column grid array is an extreme attempt to separate the package from the board. Smaller attachment pads cause a slight increase in solder joint standoff height. A reduction in the attachment pad size from 16 mils (0.4 mm) to 12 mils (0.3 mm) showed a 25% improvement in solder joint fatigue life of a flex based 0.8 mm pitch 180 I/O CSP. Figure 10, shows the Weibull distribution for the 180 I/O device. Shown in the plot of Figure 10, is the failure data for devices assembled onto a 0.062" (1.58mm) thick PCB with Cu OSP pads. The testing was performed in a -40-125C ATC. The cycle was 60 minute with 15 minute ramp and dwell times. Event detection was used to monitor first failure.

**Figure 10 - Weibull Distribution of Pad Size Effect Sample 1 0.016" (0.4mm) PCB pads (N63 906, Beta 6.1) Sample 2 0.012" (0.3mm) PCB pads (N63 1227, Beta 7.0)**



It is however possible to make the pads small enough to reduce the joint robustness. In the case of a very small pad, the failure location will shift from the component side towards the board side due to a greatly reduced solder joint

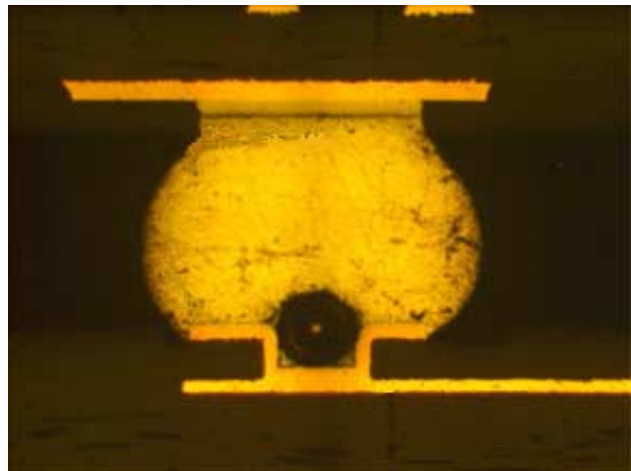
area. Shown in Figure 11, is a CSP soldered to a 6 mil attachment pad. That failed at less than 500 cycles 0-100C. Note the failure location is at the PCB side.



**Figure 11 - PCB Side Failure of CSP With 6 mil Pad**

Attachment pad design is equally important when considering assembly tradeoffs. Pad definition, mask versus pad defined geometry, will change the joint shape and stress concentrations within the solder. Mask defined geometry increases the chance of solder mask residue on the pad surface. At the solder to mask corner interface, there is a drastic increase in the stress concentration, which leads to crack initiation. Fatigue cracks generally start from the mask corner in a mask defined geometry.

Another pad design issue is the use of a via in pad structure. Assembly onto a microvia is becoming a popular alternative to fine line routing. One of the advantages of via in pad technology is the reduction or elimination of traces routed between attachment pads. This allows for a more relaxed soldermask tolerance, reduction of the possibility of exposed conductors, and larger assembly pads. However, one drawback is the fact that voids often form within the solder joint over the via structure. Figure 12, shows a CSP assembled onto a via in pad.



**Figure 12 - CSP Assembly on 6 mil Via in 12 mil pad**

In an extreme case, the void may reduce the mechanical robustness of the assembly. Filling the via with solder before assembly, or plated and filled vias may eliminate this issue. Many independent theories on the presence and formation of voids exist in literature. Most agree that voids form during the metal oxide reduction and flux outgassing stages of reflow [19, 20, 21, 22, 23]. However, voids can be formed by entrapped air, mask residue and other debris as well as contamination of the attachment pads by organic materials such as fingerprints [24].

## **2.4 Machines and Tooling**

The standard surface mount PCB assembly process sequence is sufficient for the assembly of CSP/BGAs. This sequence includes solder paste deposition, component placement, and reflow soldering. Therefore, the equipment considered in this research includes the stencil printer, the component placement machine, and the reflow oven. Also, tooling was designed and made to help achieve the desired process parameters and to facilitate the assembly process. The machines and tooling used, and their effects on assembly yield are described below.

### **2.4.1 Stencil**

Printed solder paste volume is an important process variable. It has a tremendous impact on assembly yield. Insufficient solder paste volume may result in solder opens while excessive solder paste volume increases the chances of bridging. Printed paste volume is determined by several parameters. Stencil design including aspects such as aperture condition, aperture shape, aperture size, aperture spacing, tapered edges, thickness, and fiducial deviation have a significant influence on the printed paste volume. Depending upon the stencil manufacturing process (laser cut or chemically etched apertures), the difference in the aperture wall roughness might be substantial. In order to achieve better solder paste transfer, aperture design with tapered edges should be used.

Aperture shape and size are typically dependent upon the pad design. However, over printing (where the aperture size is larger than the pad size) is not unusual when a substantial amount of paste needs to be deposited on the pad for example high lead BGAs. Overprinting is often needed for fine pitch CSPs to compensate for rather low volume transfer efficiencies found in 0.5 mm pitch CSP assembly. The aperture could be enlarged proportionally to the corresponding pad or asymmetrically (for instance, oblong apertures versus circular pads). When over printing is done, the spacing between adjacent apertures is reduced (compared to that between pads), and chance of solder balling and bridging during reflow increases. Another way to increase the solder paste volume is to increase the thickness of the stencil. However, it is difficult to print paste using a thicker stencil with small aperture sizes due to the decreased aspect ratio (aperture area divided by aperture wall area).

### **2.4.2 Stencil Printer**

The process parameters studied in the stencil printing process included the squeegee type and hardness, print speed, print pressure, and the print gap. The objective of stencil printer setup is to ensure a clean sweep on the stencil surface while ensuring a repeatable solder paste deposition process. If a polyurethane squeegee is used, squeegee hardness levels between 80 to 95 on the Shore A scale could produce appropriate and repeatable solder deposits. Print parameters such as the print speed, print pressure, and the print gap can be adjusted to accommodate the different solder paste rheologies. The setup of the printer must be reviewed and verified by domain experts.

### **2.4.3 Placement Machine**

The throughput, accuracy, and repeatability obtained from a component placement machine are a function of its design and intended application. The placement machine is usually the most expensive piece of equipment in the assembly line and its cost is proportional to the machine's features, accuracy, and repeatability. The required production rate, the pitch and size of the components to be placed, and the packaging format are some of the factors that need to be considered in selecting an adequate component placement machine. The choice of a placement machine and its capabilities is application dependent. Placement accuracy can be defined as the deviation of the center of any component lead from the center of the corresponding circuit pad. Due to the finite resolution capability of the placement machine, the target viewed by the machine is not often the actual target. Instead, the machine's target is the point of resolution nearest to the actual target and therefore placement deviation occurs. When the distribution of actual locations is established, the accuracy is the distance from the modal point of this distribution to the machine target. The repeatability is the distance from the modal point of the distribution to the point of the maximum deviation. Statistically, repeatability can be expressed as one-half the total range of the distribution. The accuracy of the placement machine is the net effect of program accuracy, component delivery, head positioning accuracy and repeatability, and vision system capabilities [25]. The placement of BGAs does not require a comparable level of accuracy in placement compared with fine pitch SMT devices. This is because area array devices usually have a coarser pitch and larger ball size. These (CSP & BGA) packages can be mechanically centered during the placement operation unlike ultrafine pitch components that require vision assisted centering. In addition, BGA packages exhibit tremendous self centering capabilities during solder reflow [26].

The types of feeders used and the size of the component can also influence placement accuracy. Larger tolerances at the feeder site where the component is located can result in a deviation of the center of the component from the actual pick-up location. The deviation on the theta axis can be exaggerated due to the larger component size [25]. In addition, the accuracy of the measuring method plays an

important role in the derived measurement. Ideally, the accuracy of the measuring method should be an order of magnitude higher than the accuracy being measured. Placement machine accuracy and repeatability in the X, Y, and  $\Theta$  axes can be measured using the precision glass slugs and precision plate approach. A statistically valid test strategy can be used to verify the machine's published specifications.

#### 2.4.4 Carrier

During the assembly process, the board (substrate) needs to be properly supported to ensure board flatness. Typically, under-board supports are provided at each work station, but are not always available in the conveyor system. When thin and/or large boards are populated with components such as CSP/BGAs, the weight of the board itself along with the weight of the components may deform the substrate in reflow and result in board sagging. This effect may shift the component from its designated location on the board after placement. Consequently, there is a large variation in solder joint height which increases the potential for solder joint defects, such as bridging and opens. In general, carriers need to be designed and used for large and/or thin boards in order to ensure proper board flatness.

#### 2.4.5 Reflow

The most popular method of reflowing solder is based on forced convection and/or IR radiation. Some other methods of solder reflow are vapor phase, laser, and hot bar. Mesh belt and edge conveyors are commonly used in reflow ovens. Critical parameters that need to be controlled in the reflow profile are the peak reflow temperature, oxygen level, dwell time above liquidous, soak time, ramp rate, cooling rate, conveyor speed, and the temperature difference across the assembly ( $\Delta T$ ).

The ramp rate in the preheat zone needs to be in a reasonable range. If the rate is too low, the assembly might not be able to reach the required soak temperature fast enough. On the other hand, if the rate is too high, components might be thermally shocked which causes failure. Proper soak temperature and soak times are required to evaporate solvents and to activate flux in the paste. The soak time has a significant influence on the temperature difference among components. The longer the small components are kept at a fixed temperature level, the better the chance that the large components can reach the same temperature level. The solder paste must be elevated to a temperature that is generally 20 to 50 degrees greater than its melting point [6]. Moreover, high reflow temperature promotes intermetallic growth and results in brittle solder joints [27]. Typically, the dwell time above liquidous is about 50-70 seconds. Long dwell time may result in dewetting and reoxidation of solder joints while short dwell time can lead to non-wetting.

### 3.0 RELIABILITY RESULTS

While there are dozens if not hundreds of factors that affect CSP assembly yields and solder joint reliability, a few

parameters stand out as being the most critical. The largest difference in CSP solder joint fatigue was found from the following parameters:

#### 3.1 Board thickness

In general, as the board thickness and overall stiffness decreases, the resulting stress the solder joint experiences decreases. As much as a 2X increase in fatigue life can be realized by assembling CSPs on a "thin board" 0.016" (0.4 mm) versus a thick board 0.062" (1.57 mm).

#### 3.2 Component Device Construction

As the effective CTE of the device is reduced, the expected life of the solder joints is reduced. As the packaging around the die is reduced, the mechanical and thermal properties of the package becomes more like that of the silicon die. Packages that have a ball side CTE that more closely matches the motherboard PCB, the less thermally induced strains occur. Thusly, laminate based CSPs show a higher expected life than flex based and ceramic based CSPs.

#### 3.3 Attachment Pad Size

PCB attachment pad size selection creates a tradeoff between assembly yields and reliability. Smaller pads generally give higher reliability while larger pads have a higher yield. Collapse of a eutectic solder ball will be limited by the wettable area of both the device and PCB pads. Surface tension of the molten solder tries to create the free energy state with the smallest value, thus a sphere. The wettable area of the attachment pads causes a truncation of the sphere. Ideally, the pads on the package and device should be the same size to allow a uniform joint shape to be formed. A 1-1 pad to device size will give the most spherical joints. The PCB routability is similarly affected by the pad diameter selection. Smaller pads give more circuit routing space. In general smaller pads give a higher joint standoff and thus a better reliability compared to joints with PCB pads larger than the device pad.

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